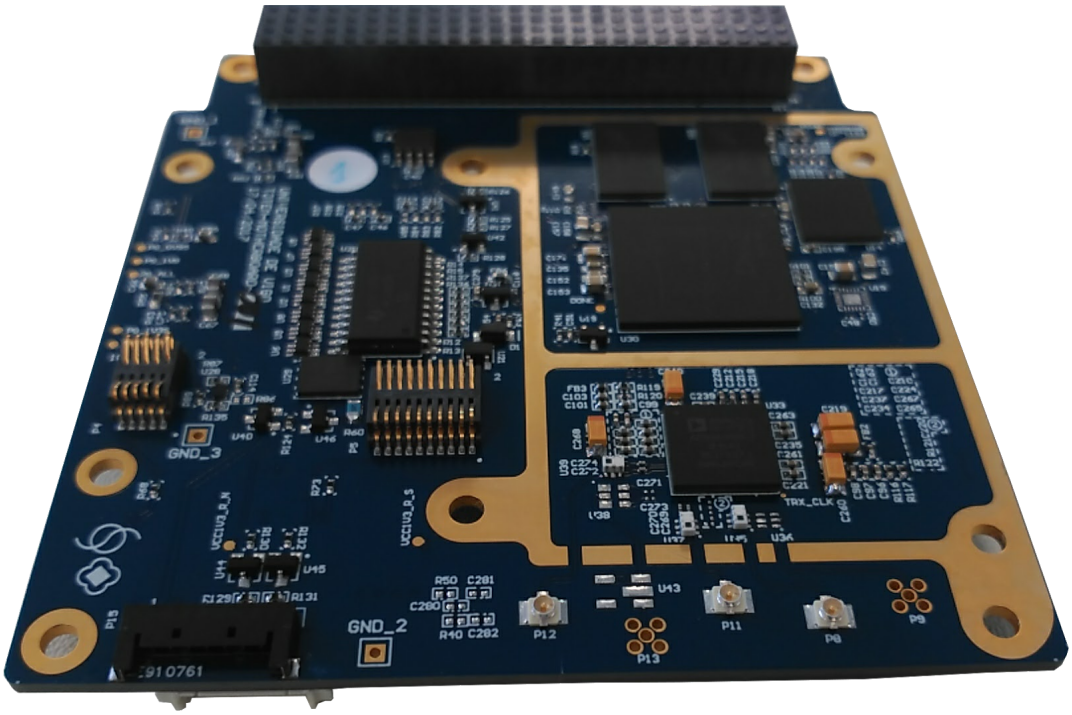

TOTEM Motherboard

Software-Defined Radio for nanosatellites

Datasheet

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1. Changelog

Table 1 - Changelog

Date	Revision	Author	Description
13/01/2018	1.0	ANV/BFA	First revision
04/12/2018	1.1	DNL	Format update
07/03/2019	1.2	DNL	Absolute Maximum Ratings System bus definition
14/06/2019	1.3	ANV	Style changed

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2. Overview

TOTEM-Motherboard is a Software-Defined Radio for nanosatellites. It is based on a high-performance System-On-Chip (Xilinx Zynq-7000 series) and a wide frequency range RF transceiver (AD9364). A FSI-connector based interface allow to easily piggy-back a custom RF frontend or TOTEM-FrontendUHF, making a full, clean and easy to integrate solution when it comes to room availability. TOTEM-Motherboard has 2 TX differential RF ports and 3 RX differential RF ports. Its modularity allows TOTEM-Motherboard to be used in many different applications.

2.1. Highlight Features

- Wideband transceiver
  - 70 MHz - 6 GHz
  - Up to 56 MHz bandwidth
  - 2 x TX and 3 x RX ports
- RF frontend as a piggyback board
- Multiple Interface
  - Ethernet, UART, JTAG, I2C, CAN
- Zynq-7020 SoC
  - Linux operating system
- 2x 4Gb DDR3L
- 8 Gb NAND Flash
- 4 Mb MRAM (SPI controlled)
- Physical properties
  - Dimensions : 89.3 mm x 93.3 mm
  - Mass: 125 g
  - PC104 Space standard
- Power supply: 5V
- Operational temperature: -40°C to 85 °C

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2.2. Block Diagram

2.2.1. TOTEM-Motherboard

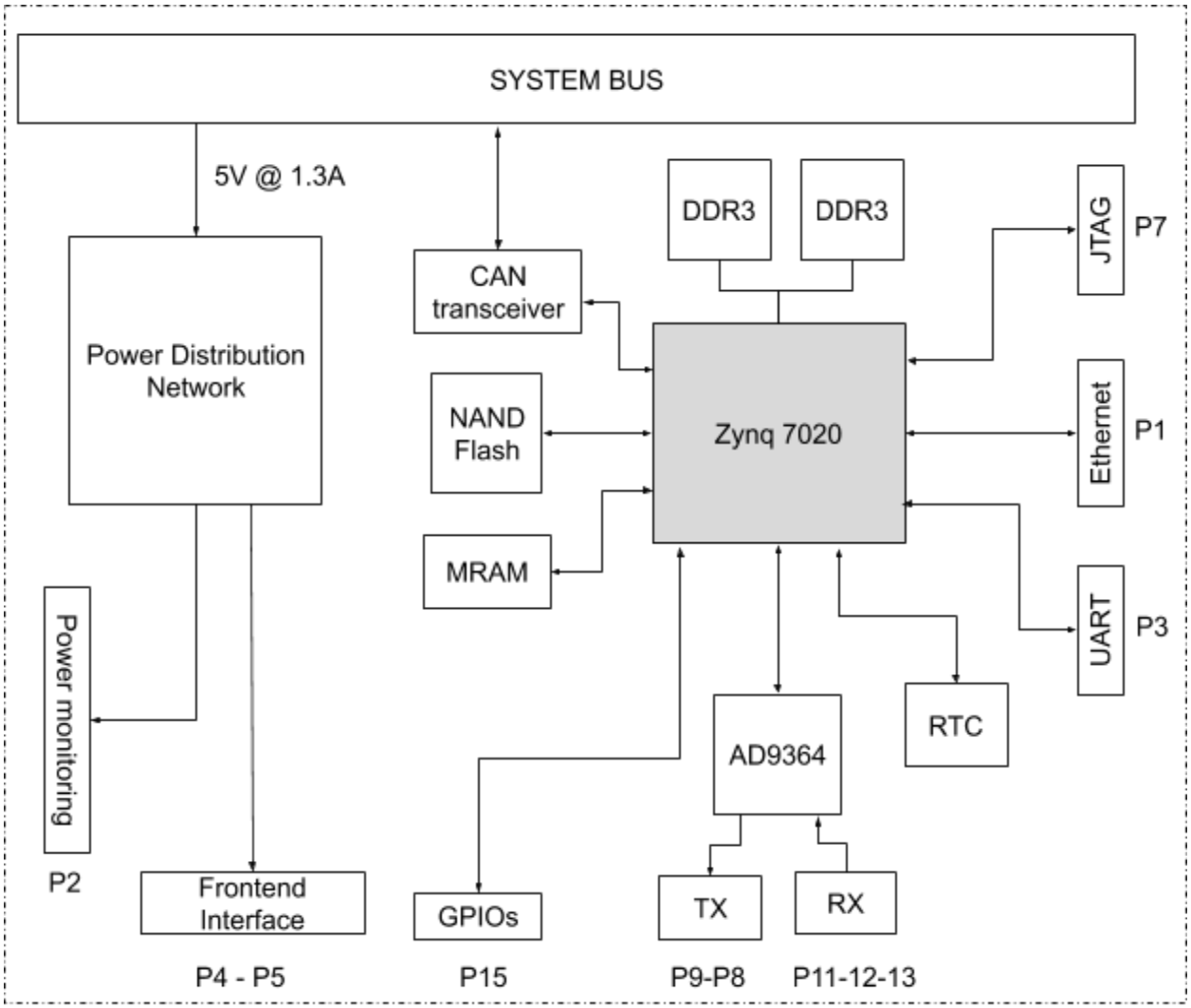

Figure 1: TOTEM-Motherboard block diagram.

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2.3. Functional Description

2.3.1. System Bus

The system bus is the connector that allows to stack TOTEM in the satellite platform, according to the PC104 Space standard. Through the system bus, TOTEM receives power (5V) and has means of communications such as CAN and I2C.

2.3.2. Power Distribution Network

TOTEM-Motherboard has its own power distribution network. Its purpose is to generate and distribute the different voltages/currents required by both TOTEM-Motherboard and the RF frontend.

2.3.3. NAND Flash

A 8Gb NAND Flash memory stores the different software images.

2.3.4. Zynq-7020

TOTEM-Motherboard core is based on a Zynq-7020, a Xilinx System On Chip (SoC) of the family Zynq-7000 All Programmable SoC. This SoC is divided in two parts : Processing System (PS) based on a dual ARM Cortex-A9 and the Programmable Logic (PL) which contains 85K logic cells with dedicated DSP slices. This merge on a single device of these two worlds join the flexibility of both software programmability and hardware acceleration implemented on the FPGA.

A Linux operating system is installed in TOTEM-Motherboard.

2.3.5. AD9364

The AD9364 is a highly integrated RF transceiver. It operates in the 70 MHz to 6.0 GHz range with a tunable channel bandwidth of 200 KHz to 56 MHz, covering most of the licensed and unlicensed bands. In transmission, the AD3964 filter and upconvert the data received by the Zynq-7020. In reception, the AD9364 filter and downconvert the data received by the RF frontend and send it to the Zynq-7020.

The AD9364 has 2 differential transmitters and 3 differential receivers. The TX outputs are connected to RF frontend through cable from TOTEM-Motherboard (P9-P11 connectors). The RX inputs are connected to TOTEM-Motherboard through a RF cable from RF frontend (P11 to P13 connectors).

The communication interface between the Zynq-7020 and the AD9364 is over a 12 bit LVDS interface (6 bit TX differential input bus with internal LVDS termination and 6 bit RX differential output bus with internal LVDS termination).

2.3.6. RF frontend interface

The RF frontend interface are two FSI connectors that allows you to easily piggy-back the RF frontend board with TOTEM-Motherboard. Through this interface, TOTEM-Motherboard will power supply and control the RF frontend. Any custom frontend can be attached to the motherboard following the RF frontend interface

Check the TOTEM-Frontend-UHF datasheet for more information about Alén Space UHF frontend.

2.3.7. Housekeeping

A complete housekeeping system is hardware implemented to monitor all currents, voltages and temperatures in both the PCB and within the SoC, allowing the user to fully control and monitor any anomaly or bad functioning of the entire board.

3. Power Supply

The Power Distribution Network (PDN) is in charge of generating and distributing the power needs for the different parts in TOTEM-Motherboard. The PDN is formed by all the power regulators, the reset circuit and the power planes that deliver the energy to each device. The voltages required by TOTEM-Motherboard are the followings:

- 0V95
- 1V3
- 1V8
- 1V35
- 2V5
- 3V3

Due to the precise power up requirements from the Zynq-7020 SoC, the power distribution needs to be properly sequenced as described in the diagram.

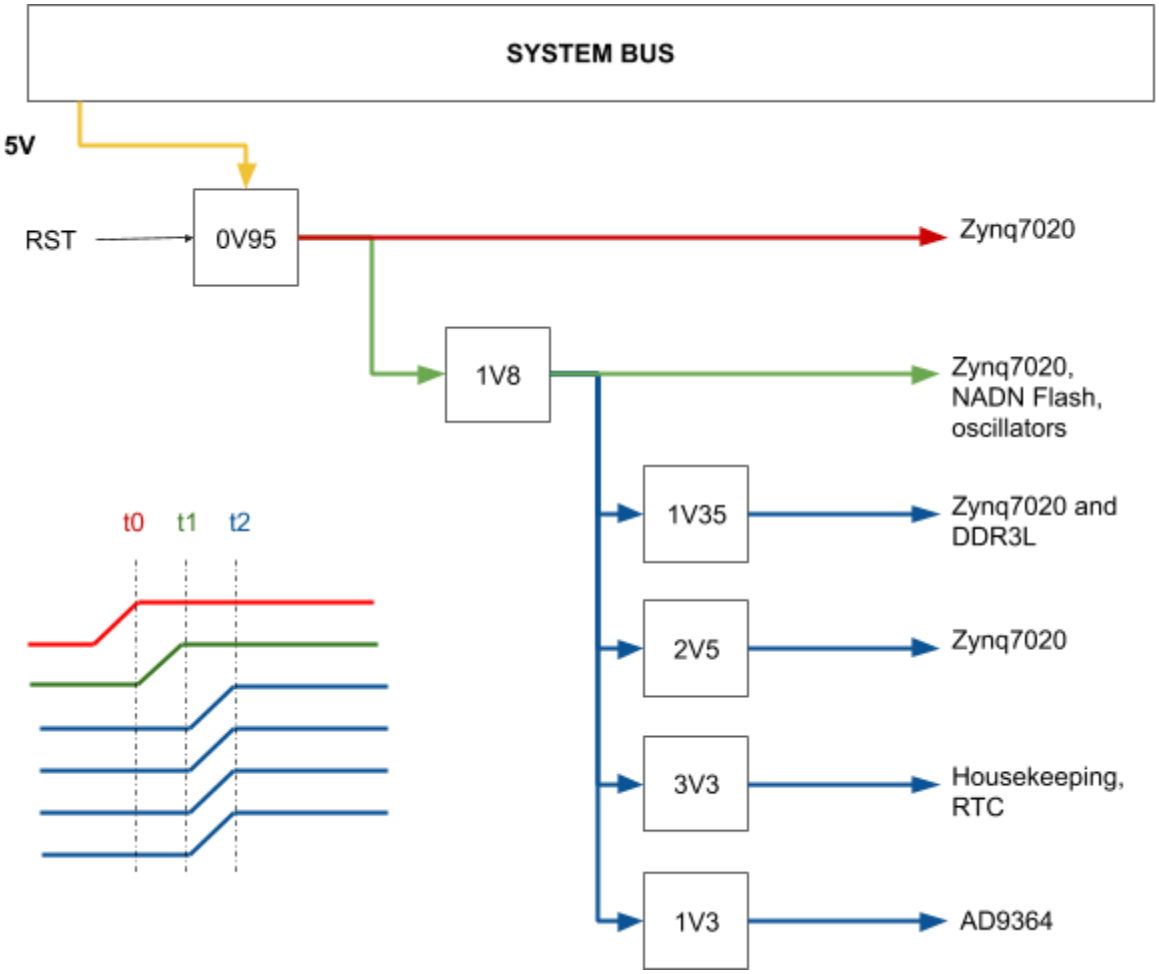

Figure 2: Power distribution network.

3.1. Reset system

TOTEM-Motherboard is able to reset itself in case of an anomaly detection. To achieve this, a dedicated reset pin in the Zynq-7020 is connected to the reset system that disconnects the power chain for 190 ms, leaving TOTEM completely unpowered. After that 190 ms gap, the power up sequence starts again.

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4. Connectors

4.1. Connectors layout

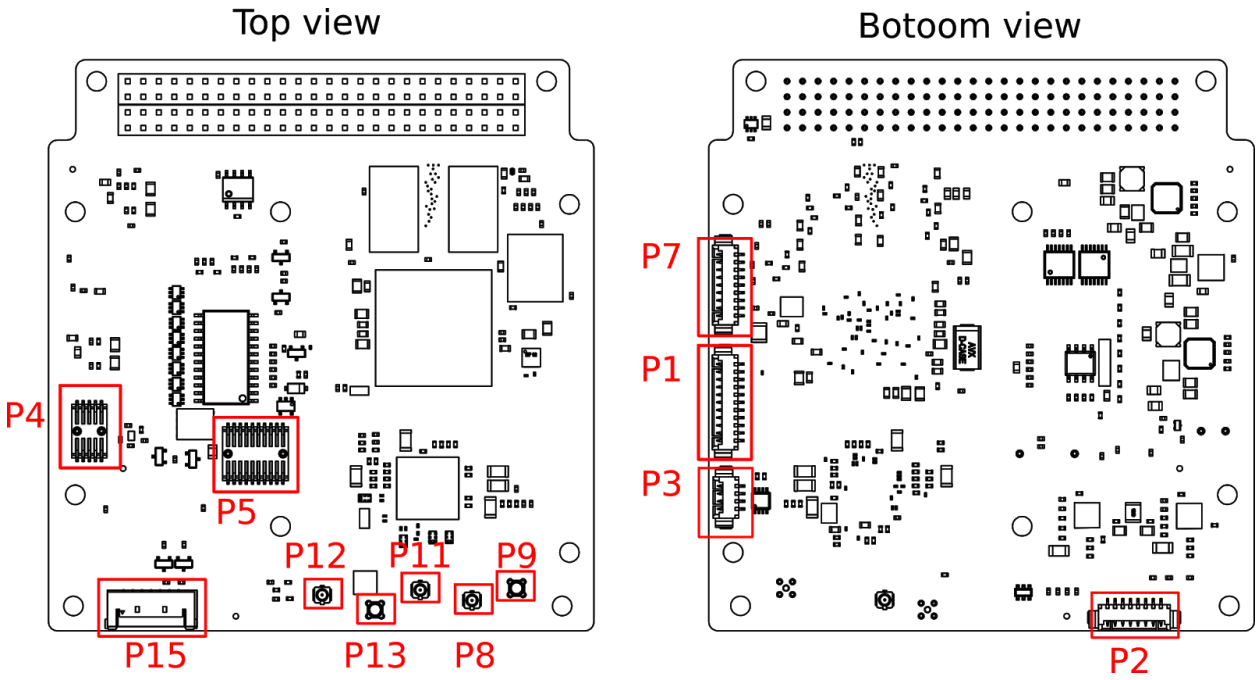

Figure 3: TOTEM-Motherboard top and bottom connectors layout.

4.2. Connectors pinout

4.2.1. System Bus

This connector is used to provide access to the satellite platform. It is composed of two 2x27-pin SSQ (SSQ-126-04-G-D) from Samtec. Other compatible connectors can be selected.

Table 2 - H1/H2 pinout

H1		H2	
Pin	**Description**	**Pin**	**Description**
1	CANL	**9 - 14**	VCC*
3	CANH	**17 - 20**	GPIOs (Note 1)
9 - 18	GPIOs (Note 1)	**25**	5V
21	SCLK (Note 1)	**26**	5V
22	MISO (Note 1)	**27**	3V3
23	MOSI (Note 1)	**28**	3V3
24	CS (Note 1)	**29**	GND
33	UART RX	**30**	GND
35	UART TX	**31**	AGND
41	SDA	**32**	GND
43	SCL	**45**	VBAT
47 - 52	VCC (Note 1)	**46**	VBAT

Note 1: These pins are customizable. Not in standard version.

Note 2: Logic levels of communications interfaces and GPIOs are TBD.

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4.2.2. P1 - Ethernet

Through the ethernet connector you can use an external ethernet module such as the Waveshare DP83848 and connect it according the following interface. Logic levels are 3V3. It is a 11-pin picoblade (53261-7011) from Molex.

Table 3.- P1 pinout

Pin	Name	Description
1	3V3	Power supply generated by TOTEM-Motherboard
2	MDIO	Management data I/O
3	MDC	Management Data Clock
4	OSC_IN	Oscillator input
5	CRS_DV	Carrier Sense/Receive Data Valid
6	RX0	Receive data
7	RX1	Receive data
8	TX_EN	TX_EN
9	TX0	Transmit data
10	TX1	Transmit data
11	GND	Ground

4.2.3. P2 – Power Monitoring

This connector will let you monitoring the main power supplies in the board. It is a 8-pin picoblade (53261-0871) from Molex.

Table 4 - P2 pinout

Pin	Name	Description
1	GND	Ground
2	VBAT	Unregulated voltage from EPS
3	3V3	TOTEM-Motherboard 3V3
4	5V	TOTEM-Motherboard 5V input power supply
5	2V5	TOTEM-Motherboard 2V5
6	0V95	TOTEM-Motherboard 0V95
7	1V8	TOTEM-Motherboard 1V8
8	1V35	TOTEM-Motherboard 1V35

Note: These voltage rails are outputs with a 100K series resistor.

4.2.4. P3 – UART

UART Debug connector. It is a 4-pin picoblade (53261-0471) from Molex.

Table 5 - P3 pinout

Pin	Name	Description
1	GND	Ground
2	3V3_VREF	3V3 reference voltage provided by TOTEM-Motherboard
3	RX (Input)	UART RX
4	TX (Output)	UART TX

4.2.5. P4 & P5 - Frontend Interface

P4 and P5 allow the connection of the Frontend piggy-back board.

P4 is a 2x5-pin FSI (FSI-105-03-G-D) from Samtec.

Table 6 - P4 pinout

Pin	Name	Description
1	GPIO1	General purpose pin I/O
2	GPIO2	General purpose pin I/O
3	GPIO3	General purpose pin I/O
4	GPIO4	General purpose pin I/O
5	DAC1	Digital to Analog converter from AD9364 CH1 (0 to 3V3)
6	DAC2	Digital to Analog converter from AD9364 CH2 (0 to 3V3)
7	GPIO5	General purpose pin I/O
8	GPIO6	General purpose pin I/O
9	GND	Ground
10	GND	Ground

P5 is a 2x10-pin FSI (FSI-110-03-G-D) from Samtec.

Table 7 - P5 pinout

Pin	Name	Description
1	5V	5V TOTE-Motherboard power supply
2	3V3	3V3 TOTEM-Motherboard generated power supply
3	5V	5V TOTE-Motherboard power supply

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4	3V3	3V3 TOTEM-Motherboard generated power supply
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GPIO1	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	2V5	2V5 TOTEM-Motherboard generated power supply
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	3V3	3V3 system power supply (not generated by TOTEM-Motherboard)
17	GPIO2	General purpose pin I/O
18	VBAT	Unregulated power supply from EPS
19	GPIO	General purpose pin I/O
20	VBAT	Unregulated power supply from EPS

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4.2.6. P7 – JTAG

Connector used for on ground programming and debugging through JTAG. It is a 4-pin picoblade (53261-0971) from Molex.

Table 8 - P7 pinout

Pin	Name	Description
1	Vref	Voltage reference provided by TOTEM-Motherboard
2	TMS	JTAG Test mode select
3	BOOT config	Boot configuration : Connect to GND to enable JTAG boot or leave it open for NAND Flash boot mode.
4	TCK	JTAG Test Clock
5	GND	Ground
6	TDO	JTAG Test Data Out
7	GND	Ground
8	TDI	JTAG Test Data In
9	PS_RST	Reset

4.2.7. P8 – TX RF connector

UF.L RF transmission connector (U.FL-R-SMT) from Hirose

Table 9 - P8 pinout

Pin	Description
1	TX RF output signal
2	GND

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4.2.8. P9 - TX RF connector

SSMCX RF transmission connector (73413-0050) from Hirose

Table 10 - P9 pinout

Pin	Description
1	TX RF output signal
2	GND

4.2.9. P11/P12 - RX RF connector

UF.L RF reception connectors (U.FL-R-SMT) from Hirose

Table 11 - P11/P12 pinout

Pin	Description
1	RX RF input signal
2	GND

4.2.10. P13 - RX RF connector

SSMCX RF reception connector (73413-0050) from Hirose

Table 12 - P13 pinout

Pin	Description
1	RX RF input signal
2	GND

4.2.11. P15 – Auxiliary connector (Defined by user)

User defined GPIO connector. It is a 7-pin pico-lock (504050-0791) from Molex.

Table 13 - P15 pinout

Pin	Name	Description
1	3V3	3V3 power provided by TOTEM-Motherboard
2	GPIO1	To be defined by the user
3	GPIO2	To be defined by the user
4	GPIO3	To be defined by the user
5	GND	Ground
6	GPIO4	To be defined by the user
7	GPIO5	To be defined by the user

5. Data Interface

5.1. CAN Bus

TOTEM-Motherboard has a CAN Bus interface routed to the system bus, allowing you to communicate with TOTEM-Motherboard compatible with CSP (Cubesat Space Protocol) packets.

CSP source code: https://github.com/libcsp/libcsp

5.2. UART

An UART interface is available for debugging through connector P3. Logic level is 3V3.

5.3. JTAG

The JTAG interface, accessible from P7 connector can be used with the Platform Cable USB II from Xilinx. This USB platform '*provides integrated firmware (hardware and software) to deliver high-performance, reliable and easy-to-perform configuration of Xilinx devices*'

Xilinx Platform Cable USB II datasheet:
https://www.xilinx.com/support/documentation/data_sheets/ds593.pdf

5.4. Ethernet

An RMII interface is configured to be accessible from connector P1. You can connect a ethernet transceiver on this port such as the DP83848 to gain network access to the SoC.

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6. Electrical characteristics

Table 14 - Electrical characteristics

Symbol	Description	Min	Typ	Max	Unit
Vcc	Supply voltage	4.7	5	5.2	V
I	Supply current	[1]	0.28	0.42 [2]	A
Pmax	Maximum power consumption	-	1.4	2.1	W

Notes:

1. Minimum current supply when power up may rise to 0.5 A.
2. Maximum current consumption in transmission mode @ 7 dBm output.

7. Absolute maximum ratings

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 15 - Absolute maximum ratings

Symbol	Description	Min	Max	Unit
Vcc	Supply voltage	3.7	6	V
VBAT	Unregulated line maximum voltage	-	26	V
Icc	Supply current	-	3	A
Temp	Operating Temperature range	-40	+85	°C

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8. Physical characteristics

Table 16 - Physical characteristics

Magnitude	Value	Unit
Size	93.3 x 89.3 x 5	mm
Mass (shielding not included)	59	g
Mass (shieldings included) [1]	130	g

Notes :

1. Shieldings in both TOP (over SoC and transceiver) and BOT (power supply chain) layers

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8.1. Mechanical drawings

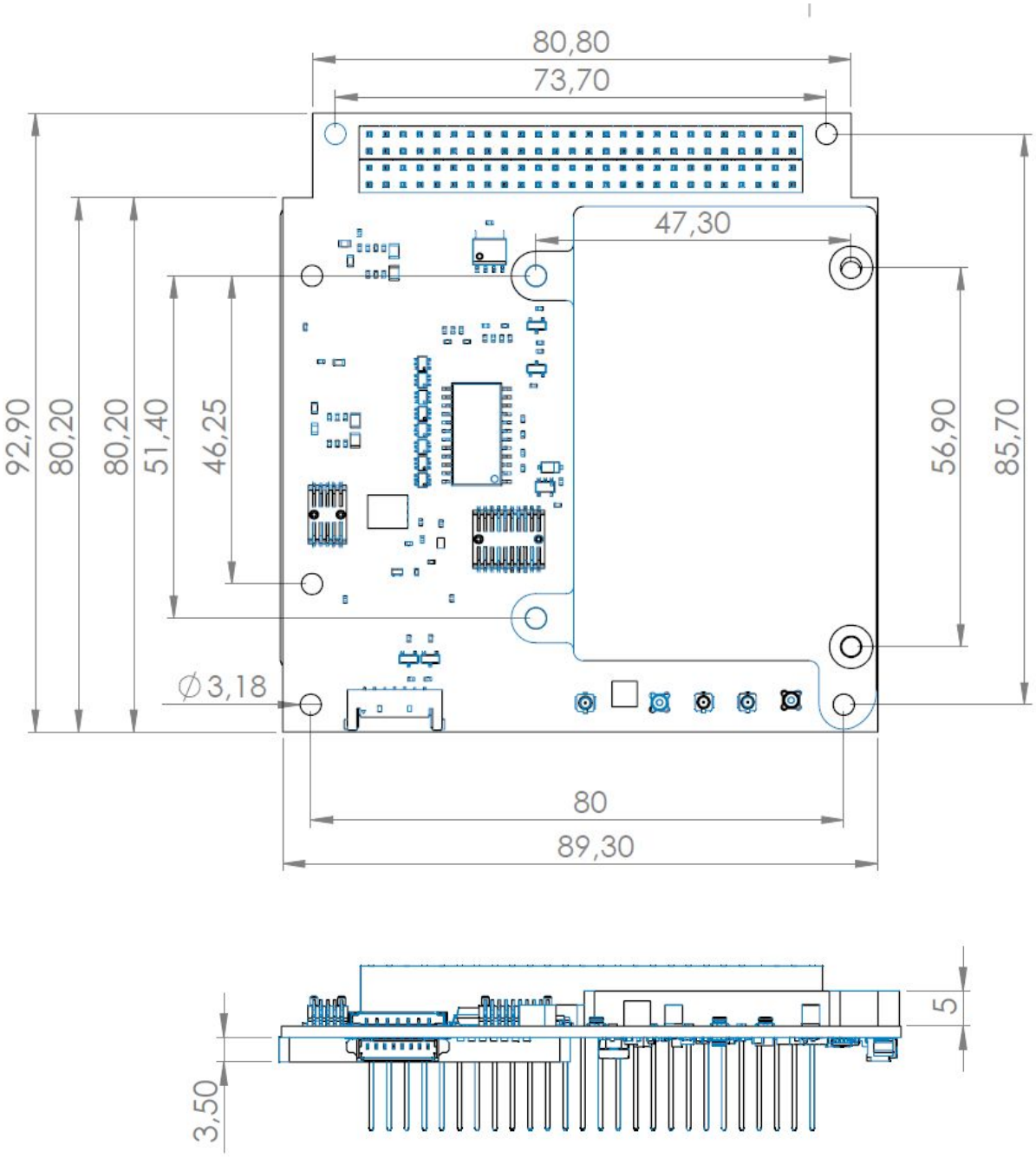

Figure 4 : Mechanical drawings