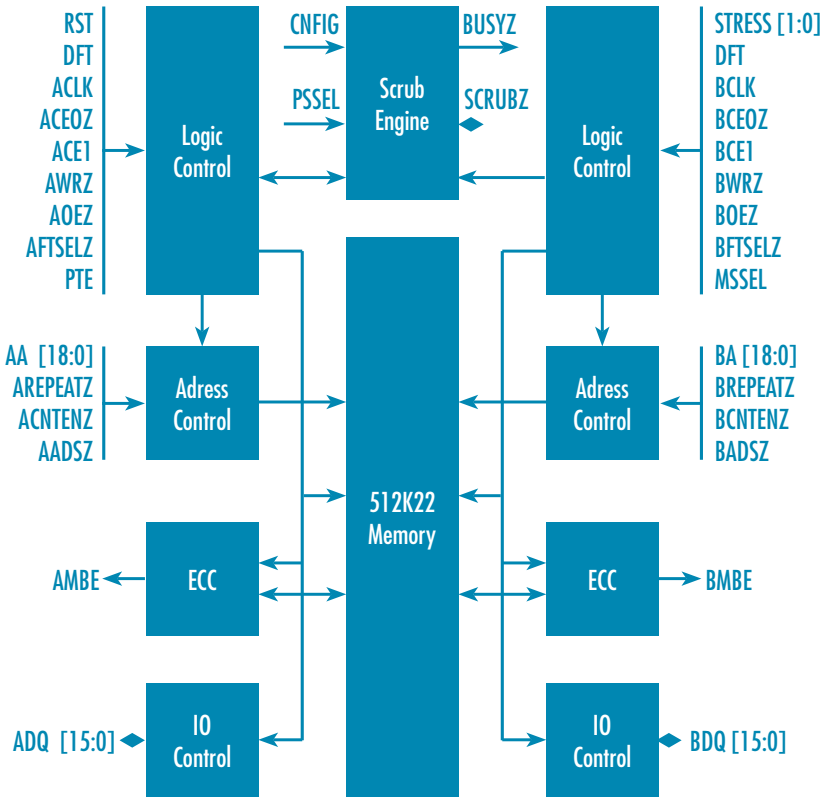
Radiation Hardened
8Mb Synchronous Dual-Port SRAM
HS512K16

VORAGO TECHNOLOGIES
Opening up new possibilities

High density 8Mb Synchronous Dual-Port SRAM manufactured with HARDSIL® technology featuring extremely low operational and standby power, latch-up immunity and on-chip EDAC.



KEY FEATURES

- Manufactured with HARDSIL® technology
- Operates as a true dual-port synchronous 8Mbit SRAM memory (512K x 16) or standard single-port 8Mbit SRAM or flexible interconnect for multi-processor environments
- Functionally compatible with commercial 512K x 16 dual-port SRAM devices
- Operating voltages
  - Core 1.5V, IO 3.3V
- Selectable pipeline and Flow-Through modes
  - Clock cycle time <20nS Flow-Through, <15nS Pipeline modeM
  - Access time <17nS Flow-Through, <12nS Pipeline mode
- Internal Error detection and correction (EDAC)
  - Single bit error detection and correction on read accesss
  - Optional background scrubbing
- Optional parity generation / checking
- Ultra low standby current < 70mA typical @ 175C
- High temperature performance >1000 hour operating life at 200C
- Package
  - 128 pin ceramic QFP
  - Die available

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RADIATION HARDENED PERFORMANCE

- TID > 300K rad (Si)
- Soft Error Rate (SER) with EDAC enabled: < 1e-15 errors / bit-day
- Latchup immunity > LET = 110 MeV-cm2 / mg (T = 125°C)

APPLICATIONS

- Industrial
- Aerospace
- Medical
- Space
- Military

Part Ordering Information

Description	Part number	Environment	Temperature Range	Package
High-temperature Synchronous Dual-port SRAM	HS512K16-CQ128A103E	Extreme temperature	-55° to 200°C	Ceramic 128 QFP
High-temperature Synchronous Dual-port SRAM	HS512K16-CQ128A1F0E	Radiation-hardened	-55° to 125°C	Ceramic 128 QFP
High-temperature Synchronous Dual-port SRAM	HS512K16-DA103E	Extreme temperature	-55° to 200°C	Die
High-temperature Synchronous Dual-port SRAM	HS512K16-DA1F0E	Radiation-hardened	-55° to 125°C	Die

HS512K16 8Mb Radiation-Hardened Synchronous Dual-Port SRAM

HS512K16 is a high performance synchronous Dual-Port SRAM organized as 524,288 words with 16-bit word. It can be configured as Master or Slave device. Master device can initiate autonomous scrub and demand scrub cycles on Slave device.

- True dual-port synchronous SRAM, 8Mb memory
- Selectable between Pipeline and Flow-Through modes
- Built-in EDAC (Error Detection and Correction) to mitigate soft errors
- Built-in Scrub Engine for autonomous correction
- Built-in Address counter for sequential memory access with repeat feature
- Dual chip enable allows depth and width expansion without additional logic
- Asynchronous Output Enable for each port
- Support various clock modes and stress test modes
- Direct read mode from data bits or parity bits for quick memory testing
- Cycle Time <20ns flow through mode, <15ns pipeline mode
  - Access time <17ns flow through mode, <12ns pipeline mode
- Manufactured by TI at DMOS5 wafer fab
- 130nm CMOS generation with commercial layout rules
- 5 levels metal, with Cu , Al layers
- 8T DP SRAM cell
- CMOS compatible input and output level, three state bidirectional data bus
  - 3.3 +/- 0.3V I/O, 1.5 +/- 0.15V CORE
- Radiation performance
  - Manufactured by TI with SST 130nm RH process and selective circuit design hardening
  - TID immunity > 300Krads (Si)
  - SER < 1e-10 errors/bit-day @ geosynchronous orbit & solar minimum (with ECC/Scrub)
  - Latch up immunity > LET = 110 MeV (T=125˚C)
- Packaging options: 128pin CQFP, Die
- Temperature options: -55˚C to 125˚C and -55˚C to 200˚C

Figure 1: Block Diagram

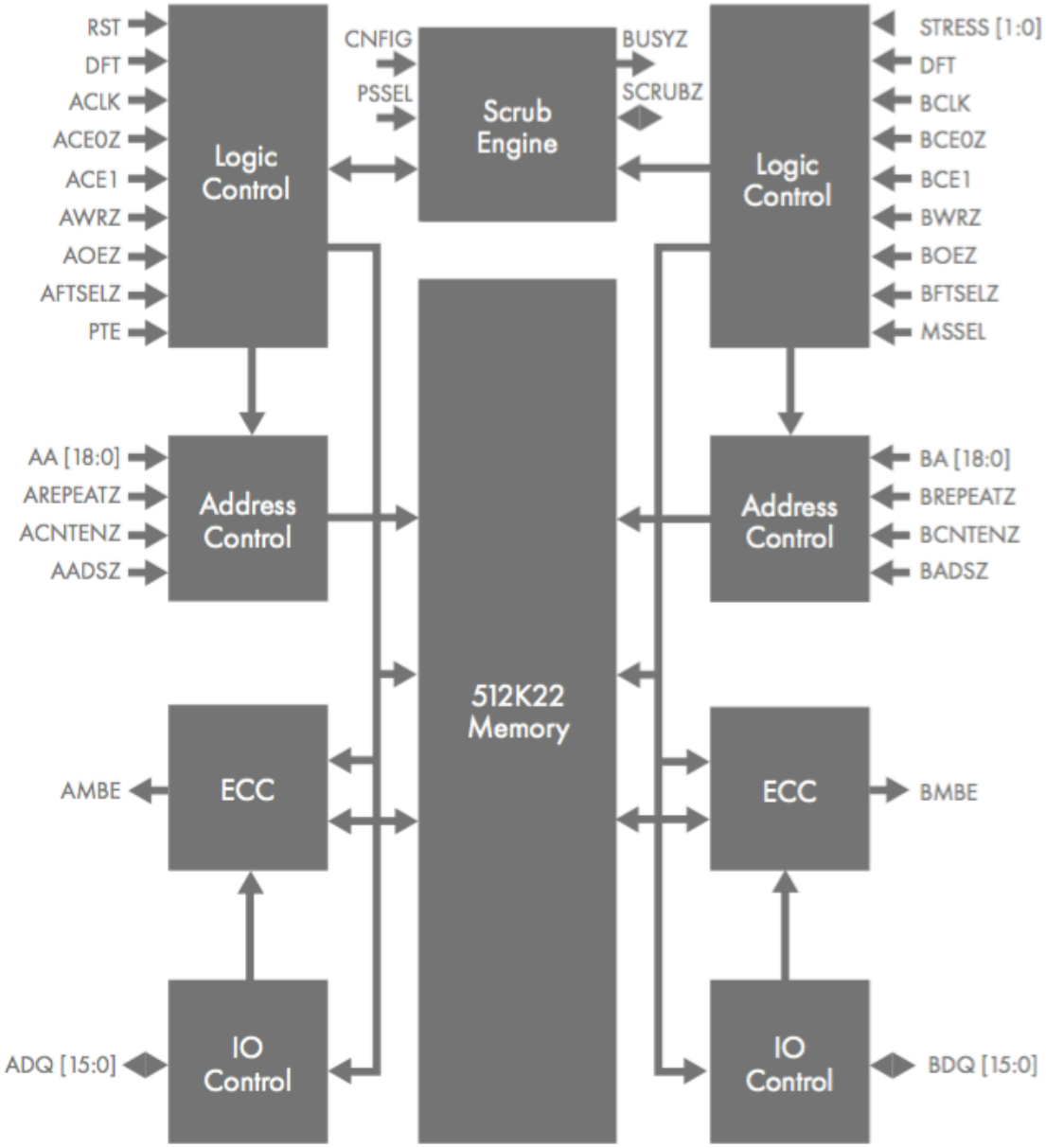


Figure 2: Pin-out

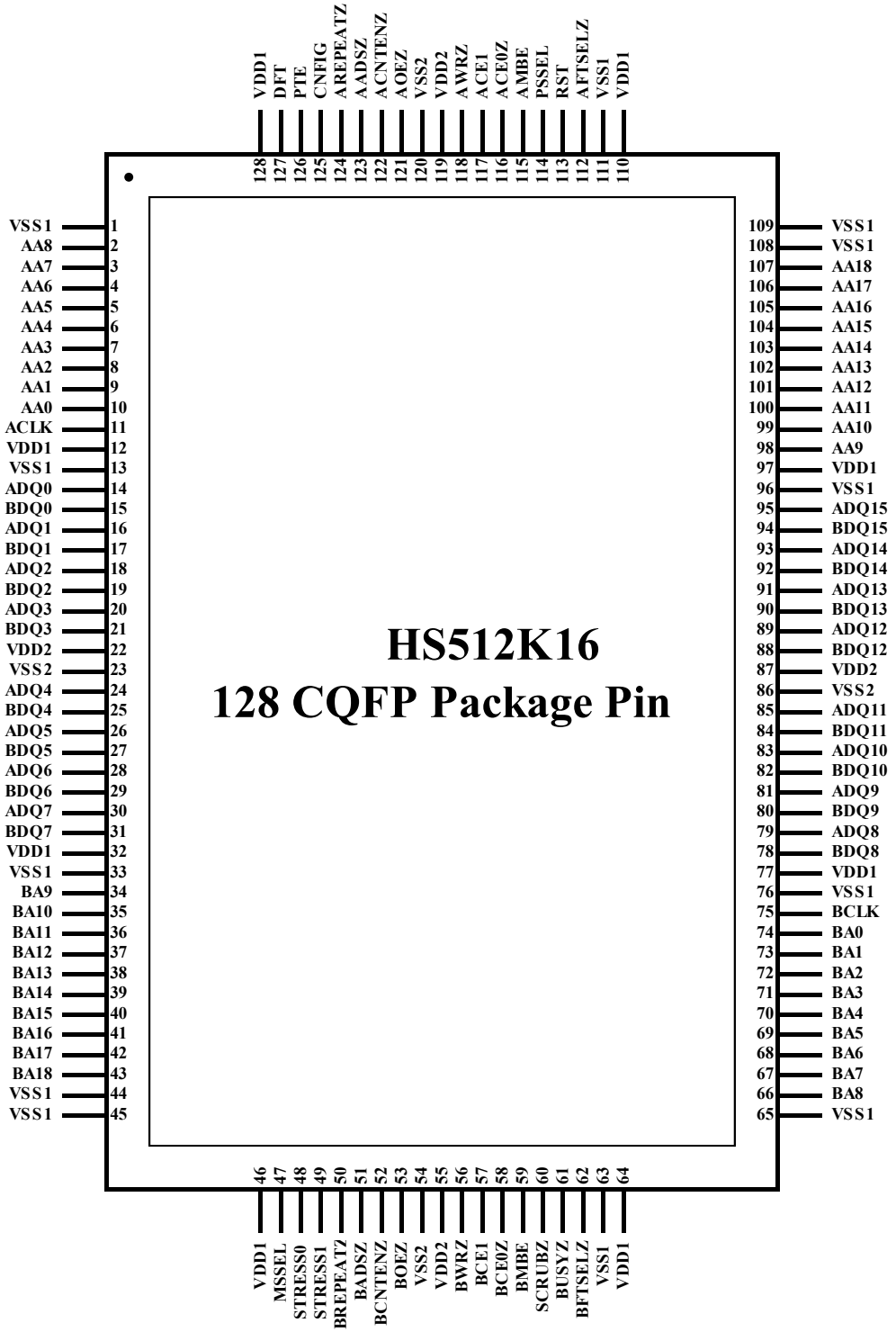


Table 1: SRAM Device Pin Description

Port-A	Port-B	Type	Active	Description
ACLK	BCLK	I		Clock signal
ACE0Z	BCE0Z	I	Low	Chip Enable-1
ACE1	BCE1	I	High	Chip Enable-2
AWRZ	BWRZ	I	Low	Write/Read Enable - Low for Write and High for Read
AA[18:0]	BA[18:0]	I		Address bus
ADQ[15:0]	BDQ[15:0]	I/O		Data bus
AOEZ	BOEZ	I	Low	Asynchronous Output Enable – Low for Read and High for Write
AFTSELZ	BFTSELZ	I	Low	Asynchronous Pipeline/Flow-Through select – High for Pipeline and Low for Flow-Through
ACNTENZ	BCNTENZ	I	Low	Port Counter Enable
AADSZ	BADSZ	I	Low	Port Counter Address Load Strobe
AREPEATZ	BREPEATZ	I	Low	Port Counter Repeat – Resets the address counter to initial address stored in Mirror Register
AMBE	BMBE	O	High	Multiple Bit Error Indicator
CNFIG		I	High	High for Configuration/Test Mode Enable – Low for Write/Read normal/Scrub mode (asynchronous)
BUSYZ		O	Low	Busy Warning; active low to indicate the scrub cycle is coming
SCRUBZ		I/O	Low	Scrub Cycle; device is not accessible when SCRUBZ is low
DFT		I	High	DFT enable; active high for portion testing (asynchronous)
PSSEL		I		Port selection for SCRUB operation; Low for Port-A and High for Port-B (asynchronous)
MSSEL		I	High	Master/Slave device selection. Low for Master and High for Slave (asynchronous). Should be treated as DC signal.
PTE		I	High	Parity Test Enable; Low for reading data and High for reading parity bits (asynchronous).
STRESS[1:0]		I		Margin Test setting: Should be treated as DC signal. + 01: normal mode; 00: screen mode + 10: slow mode; 11: very slow mode
RST		I	High	Reset Control Register to default values, prohibited the other operations. All registers defined in Table 3 are set to default values. *All internal address counter of scrub is reset to 1*
VDD2		I		Supply voltage for IO
VDD1		I		Supply voltage for CORE
VSS2		I		Ground for IO
VSS1		I		Ground for CORE

C035HS512K16 provides a true synchronous Dual-Port Static SRAM interface. Each port has its Clock (xCLK); four control inputs named Chip Enable-1 (xCE0Z), Chip Enable-2 (xCE1), Write Enable (xWRZ) and Output Enable (xOEZ); 19 address inputs xA(18:0) and 16 bidirectional data bus xDQ(15:0). xWRZ controls read and write operations. During read operation, xOEZ must be asserted low to enable the outputs and xOEZ must be asserted to high to enable the inputs during write.

- It is imperative to configure the Control Register after power up. In this operation, EDAC enable/disable, Scrub enable/disable, Scrub Rate, Delay between BUSYZ and SCRUBZ, Double Bit Error/Single Bit Error indicator, read-timing margin used in memory and external clock mode are configured. It can be re-configured whenever it is needed. Entire address bus of Port-A is used to configure the Control Register. Whenever the Control Register is configured or reset to default values, Scrub will restart to clean memory at address '0'.

Table 2: SRAM Device Control Operation for Configuration Mode

ACLK	CNFIG	AA[8]	AA[9]	AA[10]	Mode
/	H	L	L	L	Write Control Register
/	H	H	L	L	Read Control Register

Table 3: Control Register Function

Address Bits	Register	Name	Function
AA[3:0]	SRR[3:0]	Scrub Rate Register	SRR sets typical scrub frequency ($1/t_{BLBL}$, @25°C & Vdd nominal) as follows: 0 = 1.28 MHz 6 = 197 KHz 11 = 6.2 KHz 1 = 1.28 MHz 7 = 98.5 KHz 12 = 3.1 KHz 2 = 1.28 MHz 8 = 49.3 KHz 13 = 1.54 KHz 3 = 1.28 MHz 9 = 24.6 KHz 14 = 770 Hz 4 = 788 KHz 10 = 12.3 KHz 15 = 385 Hz 5 = 394 KHz SRR values of 0 - 3 are not recommended as they will result in memory unavailable to the system ~100% of the time. Default value of SRR is '7'.
AA[7:4]	SDR[3:0]	Scrub Delay Register	SDR sets the typical interval t_{BLSL} between falling edges of BUSYZ and SCRUBZ (@25°C & Vdd nominal) as follows: 0 = 60 ns 6 = 570 ns 11 = 995 ns 1 = 145 ns 7 = 655 ns 12 = 1.08 µs 2 = 230 ns 8 = 740 ns 13 = 1.16 µs 3 = 315 ns 9 = 825 ns 14 = 1.25 µs 4 = 400 ns 10 = 910 ns 15 = 1.33 µs 5 = 485 ns Minimum delay must be >25ns to insure SRAM access completed before scrub cycle starts in case of minimum delay is programmed. Default value of SDR is '0'.
AA[11]	BER	Bypass EDAC Register	0 : Enable EDAC (default value) 1 : Disable EDAC including Scrub
AA[12]	BSR	Bypass Scrub Register	0 : Enable Scrub (default value) 1 : Disable Scrub
AA[13]	ETR	Error Type Register	0 : xMBE indicate double bit error (default value) 1 : xMBE indicate singe bit error
AA[17:14]	PDR[3:0]	Pull Down Control Register **(Valid when DFT = 1)**	16 values of PDR configure the read-timing margin: 0 : 1 pull down cells 8 : 17 pull down cells 1 : 3 pull down cells 9 : 19 pull down cells 2 : 5 pull down cells 10 : 21 pull down cells 3 : 7 pull down cells 11 : 23 pull down cells 4 : 9 pull down cells 12 : 25 pull down cells 5 : 11 pull down cells 13 : 27 pull down cells 6 : 13 pull down cells 14 : 29 pull down cells 7 : 15 pull down cells 15 : 31 pull down cells Default value of PDR is '6'
AA[18]	CKR	Clock Mode Register **(Valid when DFT =1)**	0 : Self-time Mode (default value) 1 : Clock Mode

- Each port can be accessed independently with its Clock.
  - When the EDAC is enabled, 16 data bits will be encoded to 6 parity bits and these 22 bits will be written to the memory in write operation. In read operation, 22 data bits from memory will be read, decoded, corrected (if single bit error) to 16 data bits. If double bit error occurs, xMBE will be asserted to high.
  - When the EDAC is disabled, neither encoding nor decoding is executed. Only 16 data bits will be written directly into memory in write operation and 16 data bits will be read out at IO port in read operation.
- Each port can be configured to Pipeline or Flow-Through mode via xFTSELZ pin. xFTSELZ is an asynchronous signal. It should be treated as DC signal, i.e. steady state during operation.
  - Flow-Through mode is configured by putting xFTSELZ to low. In this mode, write, read operation is executed fully in one clock cycle. It requires a large cycle time (low frequency).
  - Pipeline mode is configured by putting xFTSELZ to high. In this mode, write operation completes in one clock cycle but read operation requires two continuous clock cycles. So, this mode can be used at higher frequency.

Table 4: SRAM Device Control Operation for Write/Read

xCLK	xCE0Z	xCE1	xWRZ	xOEZ	IO Mode	Memory Mode
/	H	X	X	X	Hi-Z	Standby (see Note 4*)
/	L	L	X	X	Hi-Z	Standby with enabled scrub operation
/	L	H	L	H	Data in	Word Write
/	L	H	H	L	Data out	Word Read
/	L	H	H	H	Hi-Z	Output Deselected

Notes:

1. */ : Rising edge, **L**: Low logic, **H** : High logic, **X** : Don't care*
2. *ADSZ, CNTENZ, REPEATZ are set to appropriate values for address access; refer to* ***Table 5.***
3. *DFT is set to low for normal mode and high for SRAM test mode.*
4. ***If ACE0Z = BCE0Z = H, chip will be standby WITHOUT SCRUB.***

- Each port of the memory contains an Address Counter. It allows the host access a portion of the memory sequentially. The Address Counter contains two registers: Counter Register and Mirror Register.
  - Mirror Register is used to specify the initial point of the memory that the Address Counter begins accessing. Its value is not set at power-up. A known location should be loaded into this register via xADSZ during initialization if desired. Any subsequent xADSZ access during operation will update this value.
  - Counter Register contains the address used to access a memory array beginning at the address specified by Mirror Register. This counter advances at the rising edge of xCLK while xCNTENZ is asserted. Whenever xREPEATZ is asserted, this counter is reset to the initial value stored in Mirror Register.
  - The operation of the Address Counter is independent of all memory control signals including xWRZ, xOEZ.

Table 5: SRAM Device Control Operation for Address Counter

EA	PIA	IA	xCLK	xCNTENZ	xADSZ	xREPEATZ	Mode
X	X	An	/	X	X	L	Address Counter is reset to Mirror Register's value
An	X	An	/	X	L	H	Load Mirror Register; Load Counter; External Address used
X	Ap	Ap+1	/	L	H	H	Counter enabled, Internal Address generation
X	Ap	Ap	/	H	H	H	External Address Blocked, Counter Disabled (Ap reused)

Notes:

1. */ : Rising edge, **L**: Low logic, **H** : High logic, **X** : Don't care*
2. ***EA** : External Address, **PIA** : Previous Internal Address Used, **IA** : Internal Address Used*
3. **An**: External address, Ap: Previous stored address; Ap+1: current address in counter mode
4. *Control signals are set to appropriate values for Write/Read modes; refer to **Table 4***
5. *xCE0Z low and xCE1 high for enabling address counter*

- Scrub Operation
  - Periodically, scrub engine reads and corrects every word of 512K. The whole memory will be scrubbed (cleaned) in finite duration.
  - The scrub rate can be defined by user from 0.313Hz to 1.28MHz. Note that high scrub rate will reduce memory availability (throughput).

Table 6: SRAM Device Control Operation for EDAC

xMBE	xOEZ	SCRUBZ	BUSYZ	I/O Mode	Mode
H	L	H	H	Read	Error Data (**), Corrected Error bit if it is single error, Uncorrectable Error bit if it is double error
L	L	H	H	Read	Valid Data Out (**)
X	X	H	H	X	Device Ready
X	X	H	L	X	Device Ready/Early Scrub Request Coming

X	X	L	X	Not Accessible	Scrubbing - Device Busy

Notes:

xMBE is only valid in EDAC operation modes (Read with EDAC enable or Scrub by Port-A or Port-B).

xMBE indicates Double Bit Error if ETR bit in the Control Register is '0'.

xMBE indicates Single Bit Error if ETR bit in the Control Register is '1'.

"X": is defined as "don't care" condition.

Table 7: AC Electrical Characteristics

Datasheet

Temp=125C, Vdd1=1.35V, Vdd2=3V		Flow-Through						Pipeline						Configuration Register			
		EDAC Disabled mode 0			EDAC Enabled mode 1			EDAC Disabled mode 4			EDAC Enabled mode 2			mode 3			
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Min**	**Typical**	**Max**	**Min**	**Typical**	**Max**	**Min**	**Typical**	**Max**	**Min**	**Typical**	**Max**	**Unit**
Clock cycle	T_{chch}	20			20			15			15			15			ns
Clock high pulse width	T_{chcl}	5			5			5			5			5			ns
Clock low pulse width	T_{clch}	5			5			5			5			5			ns
Address setup time	T_{avch}	5			5			5			5			5			ns
Address hold time	T_{chax}	0.5			0.5			0.5			0.5			0.5			ns
Chip Enable setup time	T_{cvch}	5			5			5			5			5			ns
Chip Enable hold time	T_{chcx}	2			2			2			2			2			ns
Write / Read Enable setup time	T_{wvch}	2			2			2			2			2			ns
Write / Read Enable hold time	T_{chwx}	0.5			0.5			0.5			0.5			0.5			ns
Data input setup time	T_{dvch}	1.5			2.5			1.5			2.5			2.5			ns
Data input hold time	T_{chdx}	1.5			1.5			1.5			1.5			1.5			ns
xADSZ setup time	T_{asvch}	4			4			4			4			4			ns
xADSZ hold time	T_{chasx}	0.5			0.5			0.5			0.5			0.5			ns
xCNTENZ setup time	T_{cevch}	4			4			4			4			4			ns
xCNTENZ hold time	T_{chcex}	0.5			0.5			0.5			0.5			0.5			ns
xREPEATZ setup time	T_{rpvch}	4			4			4			4			4			ns
xREPEATZ hold time	T_{chrpx}	0.5			0.5			0.5			0.5			0.5			ns
Access time from Clock high	T_{chqv}			16			17			12			12			16	ns
Output hold time from Clock high	T_{-chqx}	6			6			6			6			6			ns
Clock high to xMBE valid	T_{chmv}						17						12				ns
Clock high to xMBE change	T_{chmx}				6						6						ns
Access time from Output Enable low.	T_{olqv}			8			8			8			8			8	ns
Output Enable high to Data Output High-Z	T_{ohqz}			5			5			5			5			5	ns
Output Enable low to Data Output change	T_{olqx}			6			6			6			6			6	ns
Access time from Flow-Through enable	T_{ftvqv}			6			6			6			6			6	ns
Output hold time from Flow-Through enable	T_{ftvqx}			4			4			4			4			4	ns
Flow-Through enable to xMBE valid	T_{ftvmv}			5			5			5			5			5	ns
Flow-Through enable to xMBE change	T_{ftvmx}			5			5			5			5			5	ns
Chip Enable turn off to output tri-state	T_{civqz}			5			5			5			5			5	ns
Chip Enable turn on to output change	T_{civqx}			5			5			5			5			5	ns
xOEZ setup time with Clock	T_{ovch}	9			9			9			9						ns
xOEZ hold time with Clock	T_{chox}	0.5			0.5			0.5			0.5						ns
Clock-to-Clock Offset (clock skew Write-Read)	T_{chchs1}	7			7			7			7						ns
Clock-to-Clock Offset (clock skew Read-Write)	T_{chchs2}	7			7			7			7						ns

Notes:

1. All timings are used for both ports where applicable.
2. Flow-Through parameters are applied when xFTSELZ set to low for that port
3. Pipeline parameters are applied when xFTSELZ set to high for that port.
4. Conditions: Temperature = 125C, V_{dd1} = 1.35V, V_{dd2} = 3V
5. SLEW: 2.0ns, Load: 5pF

* The clock-to-clock offset is minimum delay required between clocks when both ports access same location with one port Write and the other Read or vice versa. Violation of this timing creates uncertainty in Read port Data Out, which can be old data, new data or combined of old and new data. See Timing Waveform 4.

Table 7: AC Electrical Characteristics (continued)

Temp=125C, Vdd1=1.35V, Vdd2=3V		Flow-Through						Pipeline						Configuration Register			
		EDAC Disabled			EDAC Enabled			EDAC Disabled			EDAC Enabled						
		mode 0			mode 1			mode 4			mode 2			mode 3			
Parameter	Symbol	Min	Typical	Max	Min	Typical	Max	Min	Typical	Max	Min	Typical	Max	Min	Typical	Max	Unit
BUSYZ low to SCRUBZ low (SDR = 0, SRR = 7)	T_{blsl}					70						70					ns
BUSYZ low to BUSYZ low (Scrub Cycle) (SDR = 0, SRR = 7)	T_{blbl}					12400						12400					ns
SCRUBZ low to SCRUBZ high	T_{slsh}					420						420					ns
SCRUBZ high to BUSYZ high	T_{shbh}					110						110					ns
SCRUBZ low to xMBE valid (flow-through)	T_{slmv}					200						200					ns
SCRUBZ high to xMBE change	T_{shmx}					8						8					ns
CNFIG setup time with Clock	T_{cfvch}													6			ns
CNFIG hold time with Clock	T_{chcfx}													3			ns
Read Register access time	T_{chqv3}															11	ns
Read Register output hold time	T_{chqx3}													4			ns
Chip enable turn off to BUSYZ high	T_{civbh}						10						10				ns
Chip enable turn off to SCRUBZ high	T_{civsh}						15						15				ns
MSSEL high to BUSYZ high. (Slave mode)	T_{mhbh}						9						9				ns
Config low to BUSYZ low (Tini)	T_{cflbl}						130						130				ns
Config high to BUSYZ high	T_{cfhbh}						9						9				ns
Config high to SCRUBZ high	T_{cfhsh}						13						13				ns
SCRUBZ low to output tri-state	T_{slqz}						3						3				ns
Pulse width of RST	T_{pwrst}				5												ns

Notes:

1. All timings are used for both ports where applicable.
2. Flow-Through parameters are applied when xFTSELZ set to low for that port.
3. Pipeline parameters are applied when xFTSELZ set to high for that port.
4. Conditions: Temperature = 125C, V_{dd1} = 1.35V, V_{dd2} = 3V
5. SLEW: 2ns, Load: 5pF

Table 8A: Typical Scrub Rate percent change vs temperature & supply voltage (compared to 25°C & nominal Vdd)

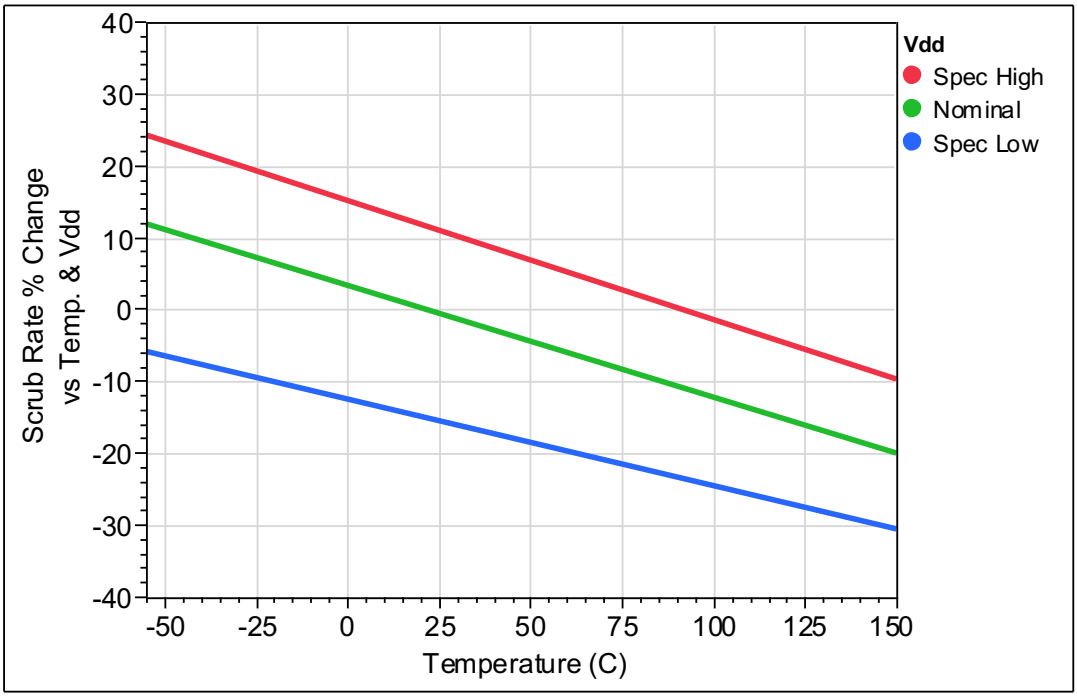
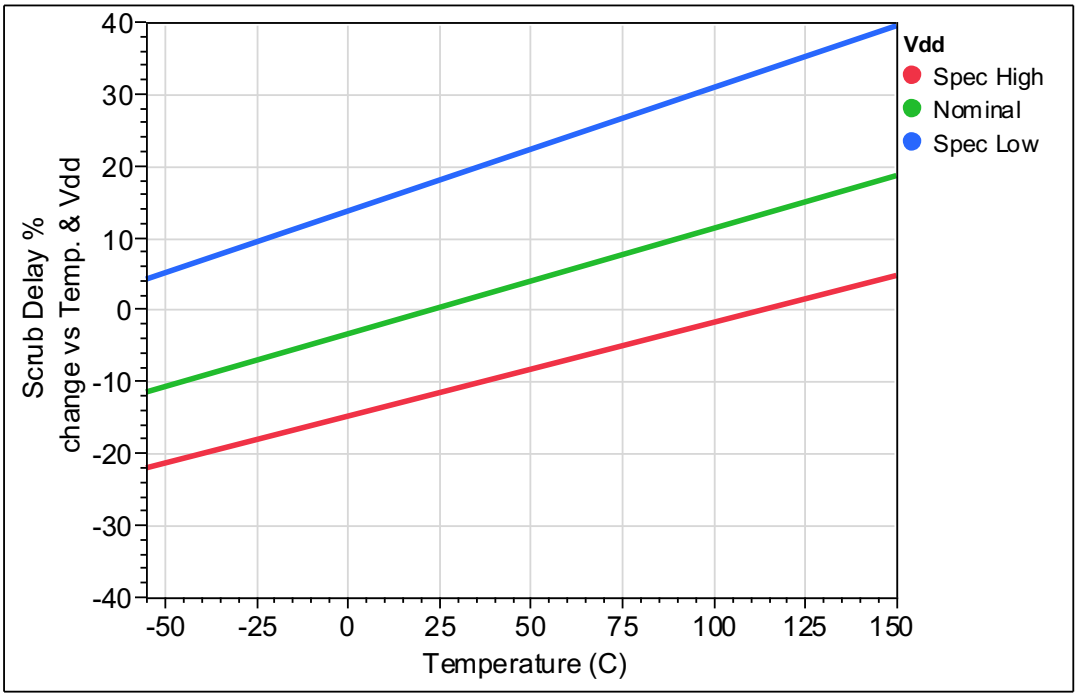
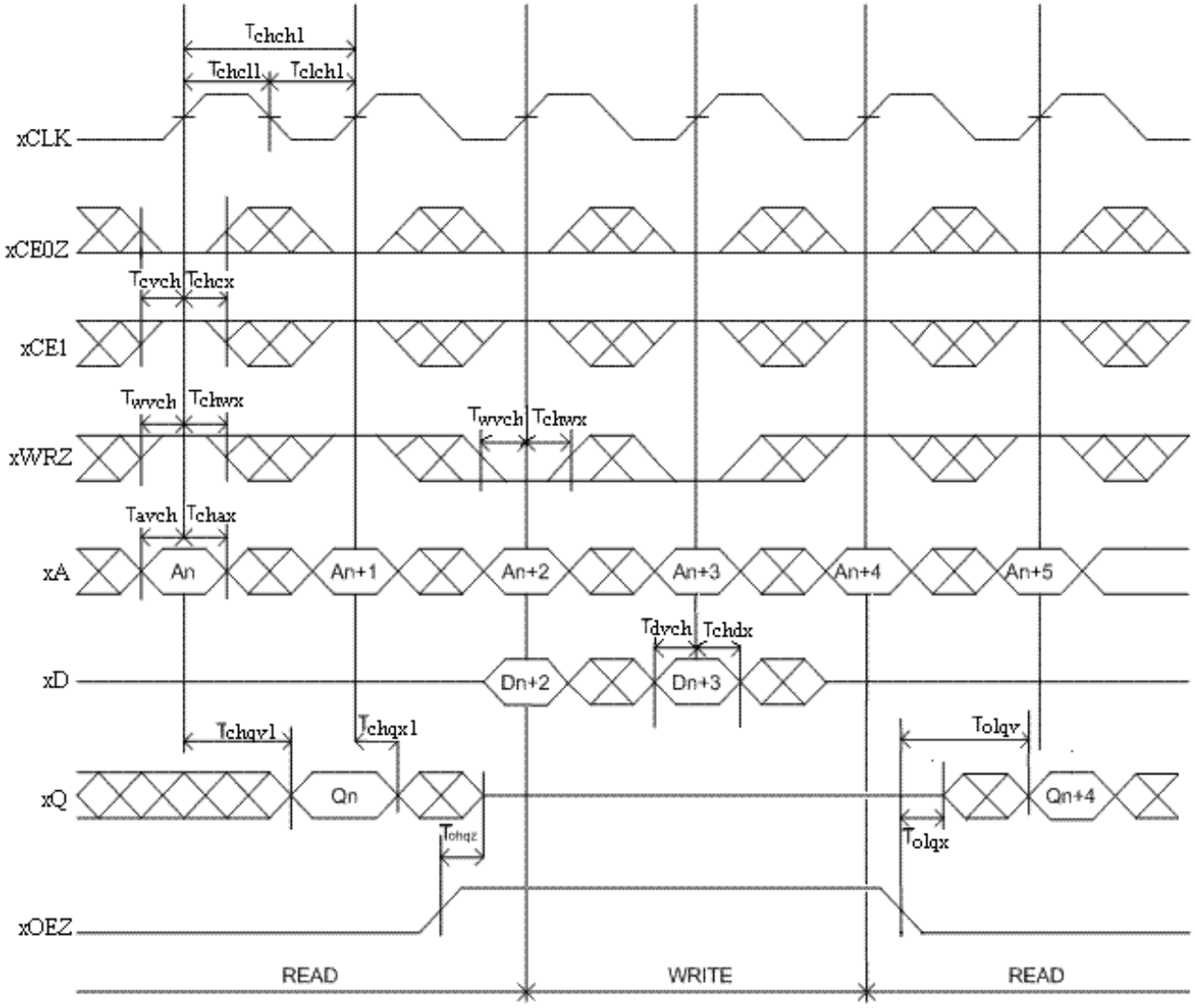


Table 8B: Typical Scrub Delay percent change vs. temperature & supply voltage (compared to 25°C & nominal Vdd)



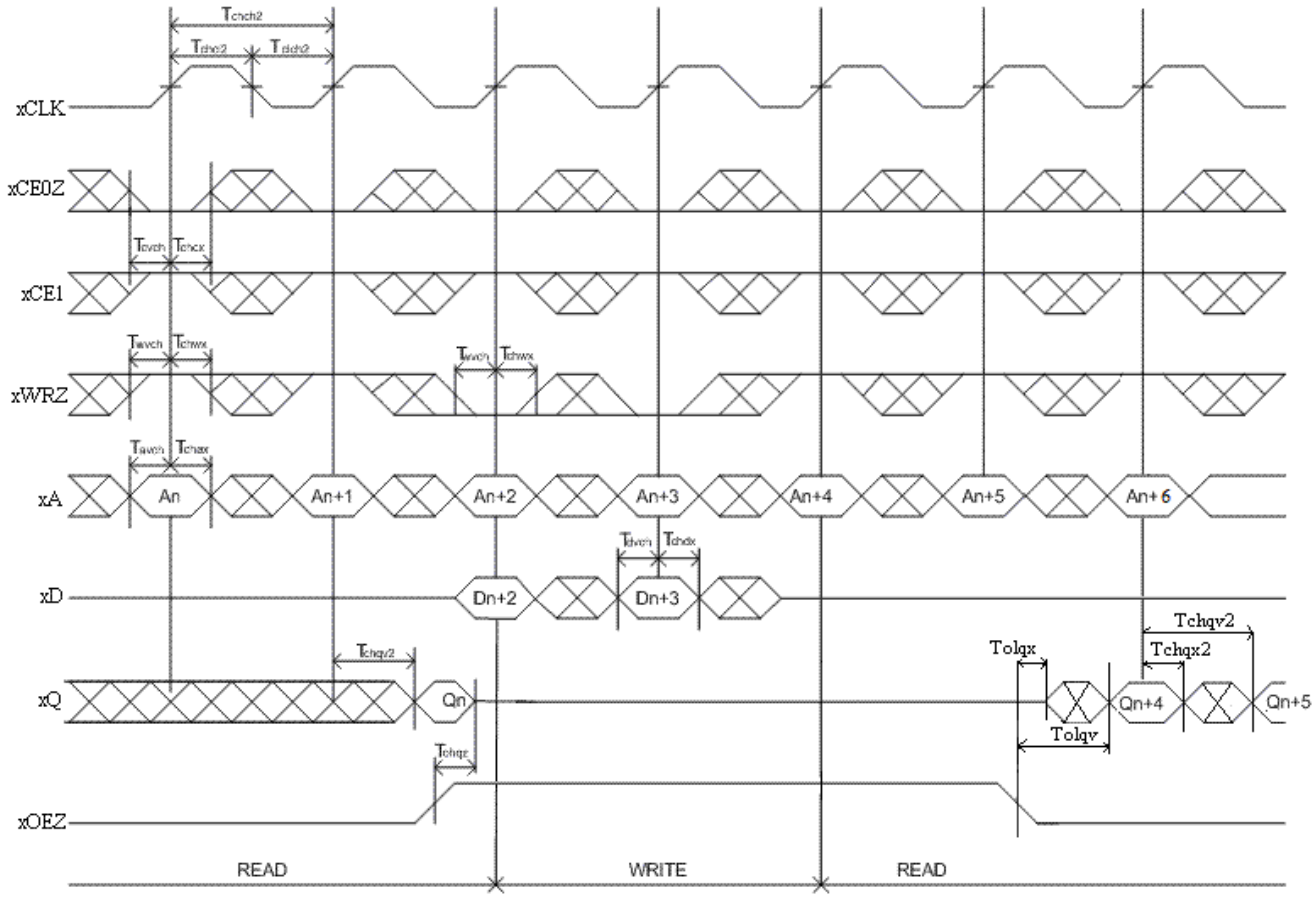
Timing Waveform1: Flow-Through (mode 0, 1) Read-to-Write-to-Read



Notes:

1. Output state (High, Low or High-impedance) is determined by previous cycle control signals.
2. xADSZ is set to low for external address using.

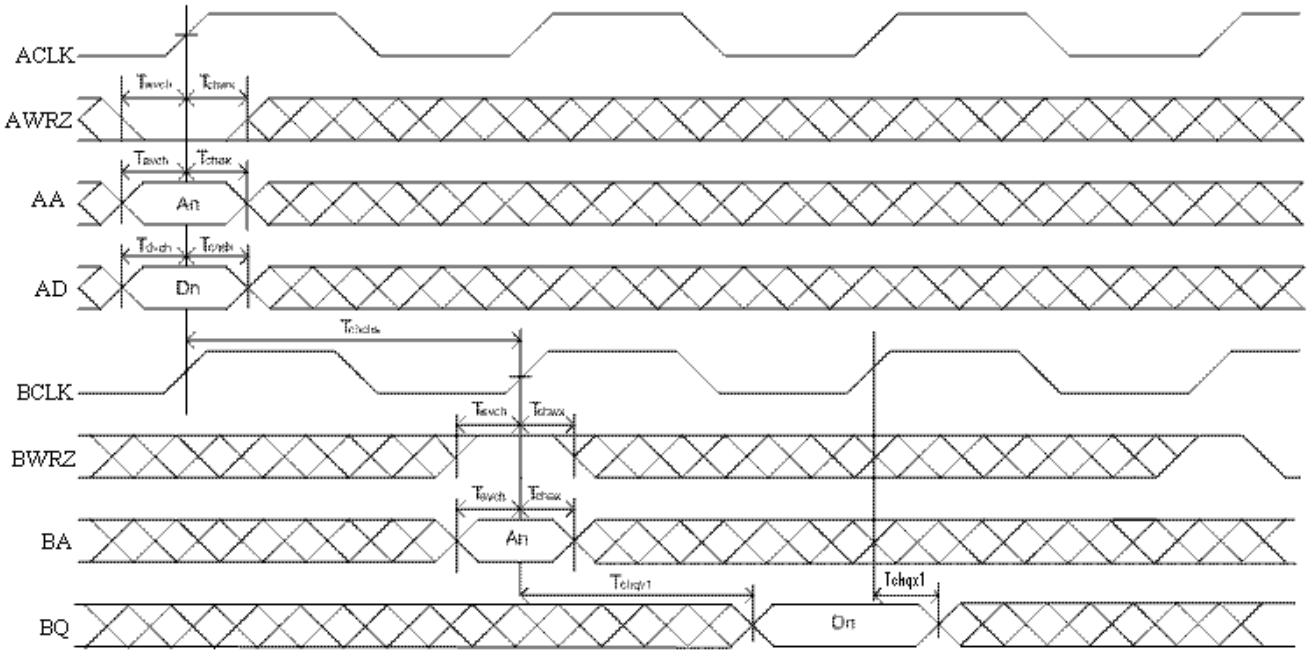
Timing Waveform 2: Pipeline (mode 2, 4) Read-to-Write-to-Read



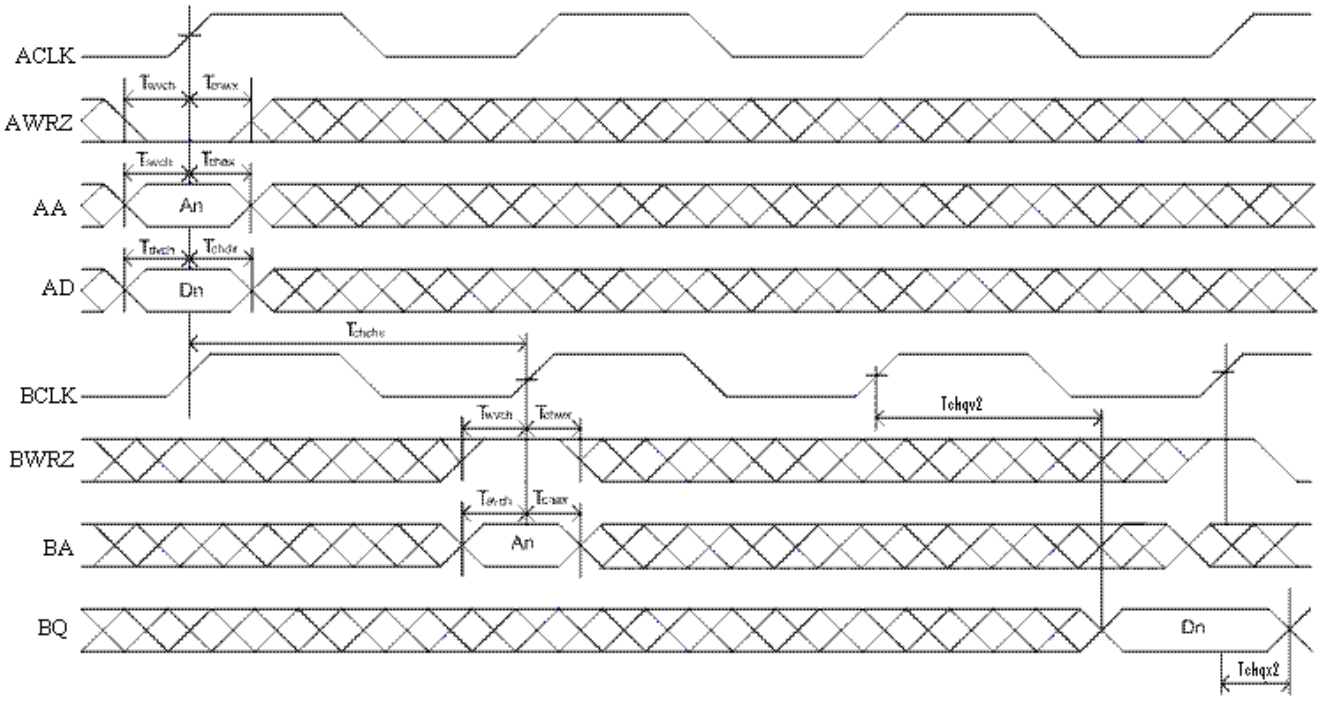
Notes:

1. Output state (High, Low or High-impedance) is determined by previous cycle control signals.
2. xADSZ is set to low for external address using.

Timing Waveform 3: Port "A" Write to Port "B" Read Flow-Through (mode 0, 1) (at the same address)



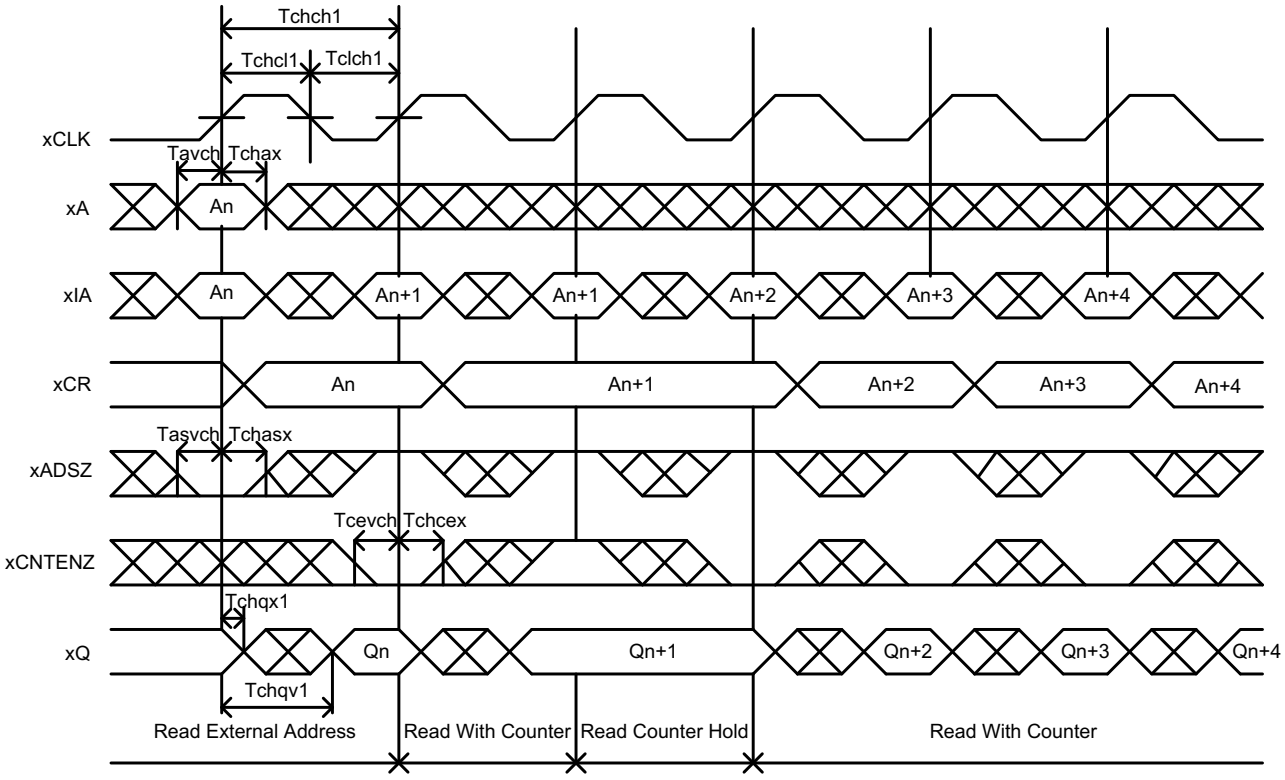
Timing Waveform 4: Port "A" Write to Port "B" Read Pipeline (mode 2, 4) (at the same address)



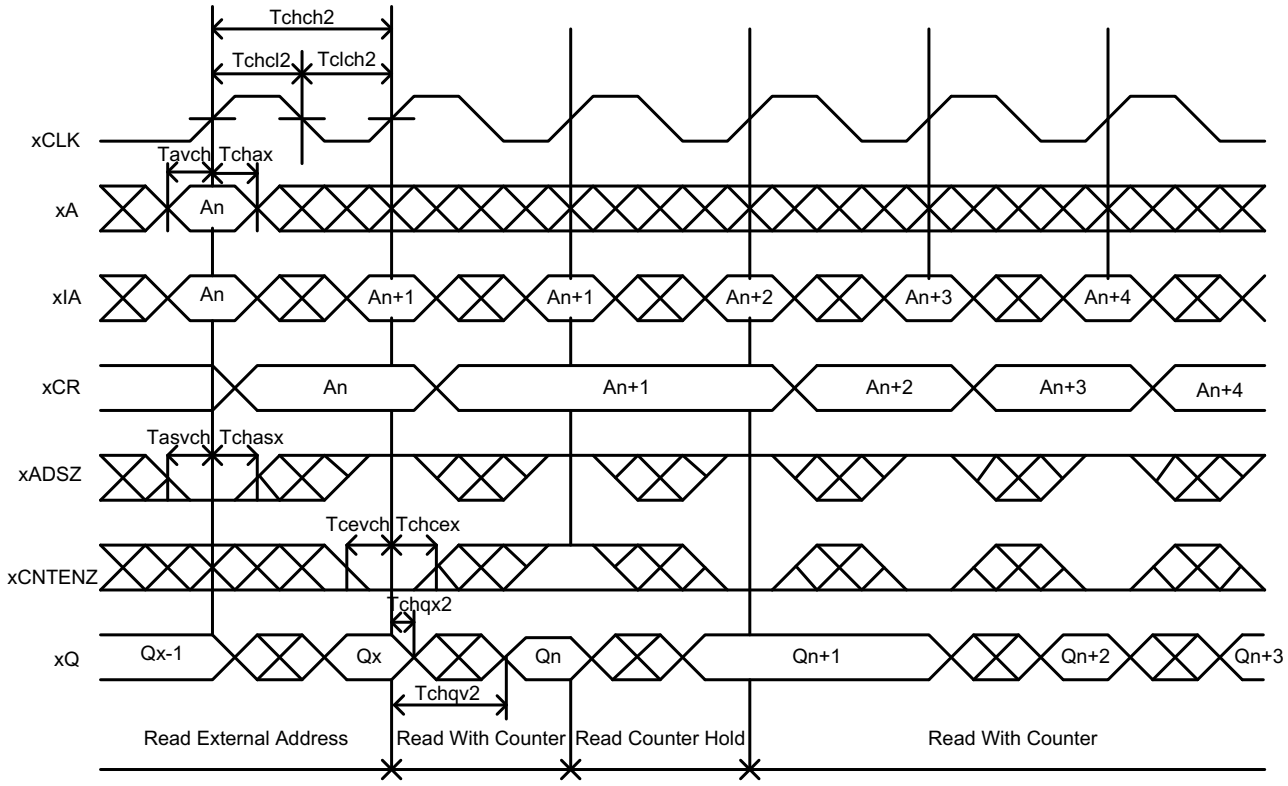
Notes:

1. xCE0Z and xADSZ are set to low; xCE1, xCNTENZ and xREPEATZ are set to high.
2. BOEZ is low for Port "B" when Port B is reading, AOEZ is set to high for Port "A" when Port A is writing.
3. If T_{chchs} < minimum specified value, then the data from read port is not valid.
4. All timings are the same for both ports.

Timing Waveform 5: Read Flow-Through (mode 0, 1) with Address Counter Advance



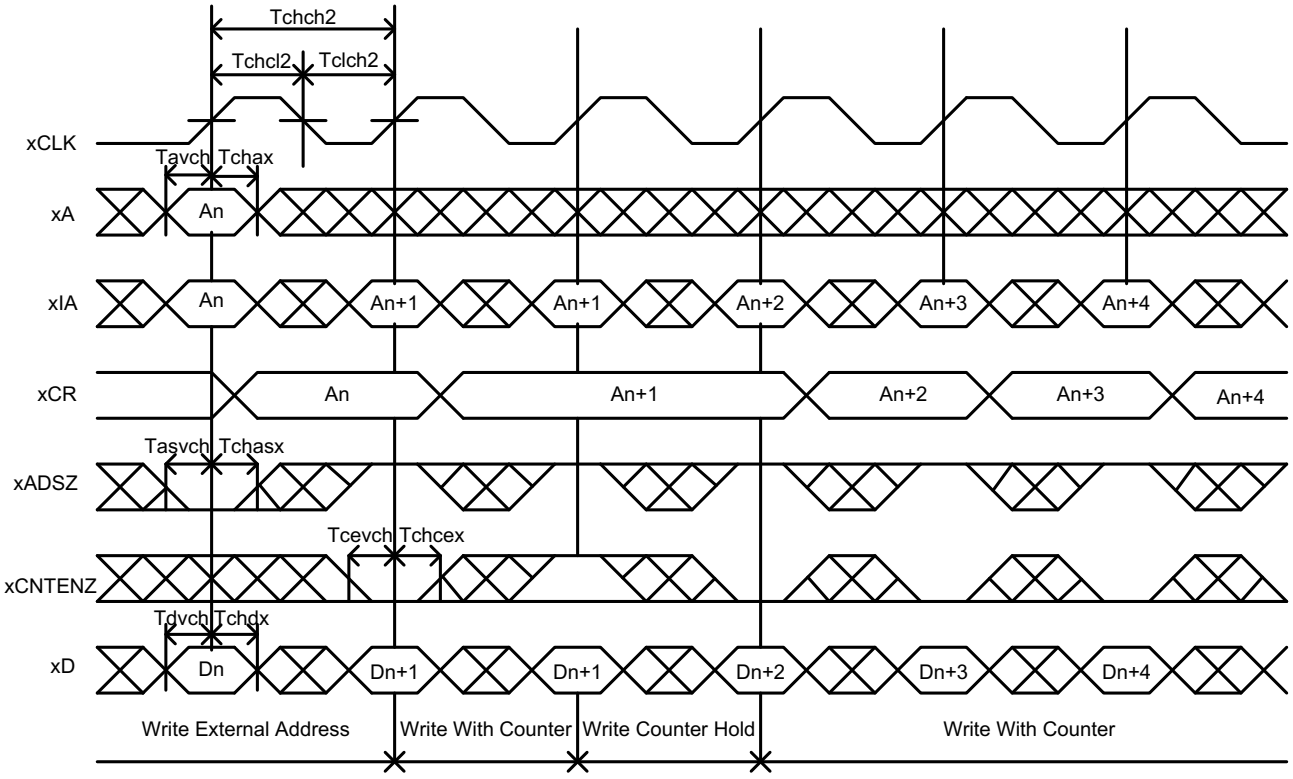
Timing Waveform 6: Read Pipeline (mode 4, 2) with Address Counter Advance



Notes:

1. xCE0Z, xOEZ are set to low; xCE1, xWRZ, xREPEATZ are set to high.
2. If there is no address change via xADSZ = Low (loading a new address) or xCNTENZ = Low (advancing the address), i.e. xADSZ = High and xCNTENZ = High, then the data output remains constant for subsequent cycles.
3. xIA: used Address for Write/Read operation of memory
4. xCR: Counter Register

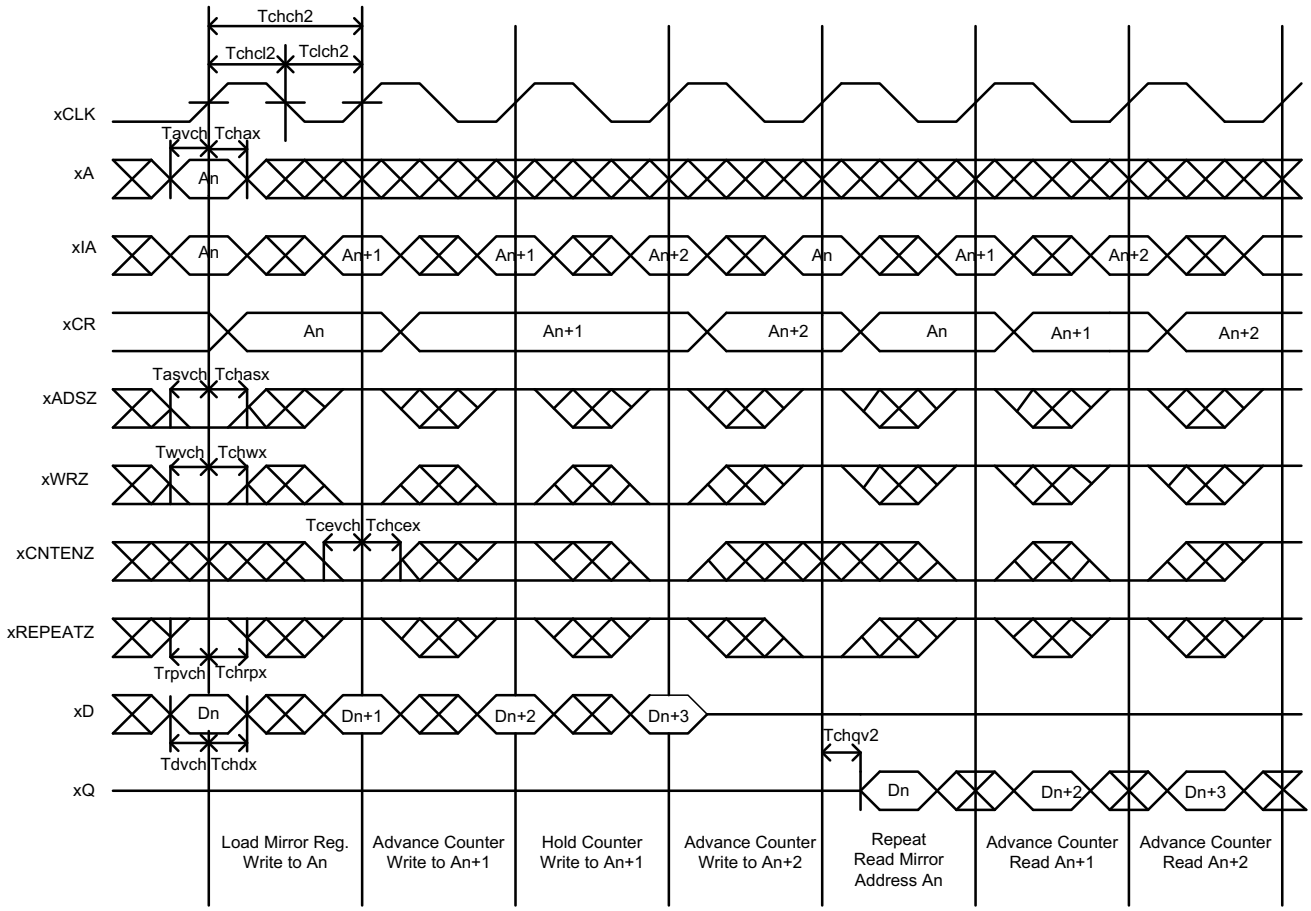
Timing Waveform 7: Write with Address Counter (Flow-through/Pipeline, (modes 0, 1, 4, 2))



Notes:

1. xCE0Z, xWRZ are set to low; xCE1, xOEZ, xREPEATZ are set to high.

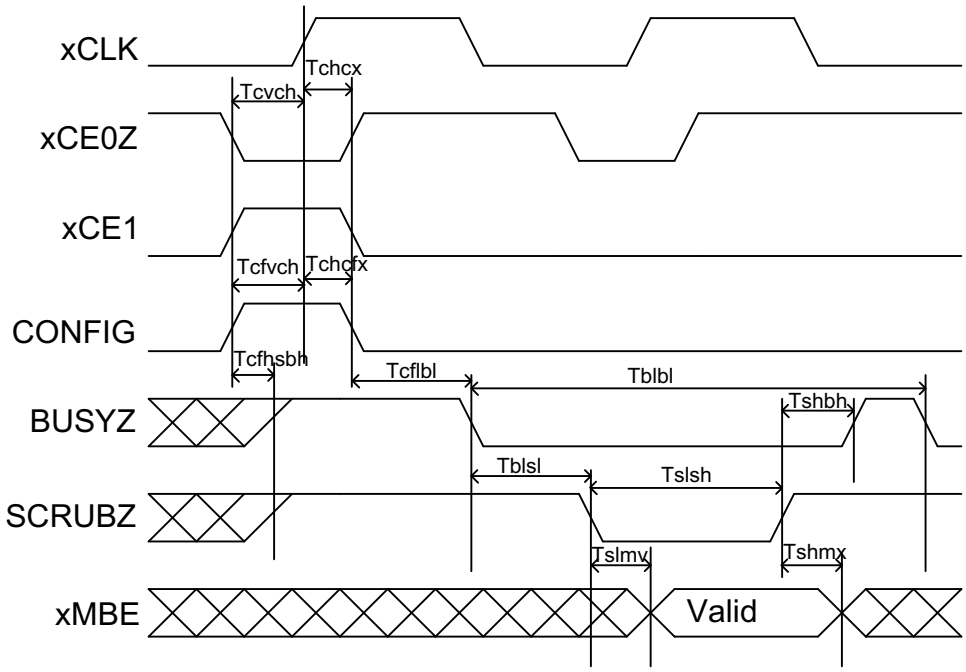
Timing Waveform 8: Counter Repeat



Notes:

1. xCE0Z is set to low; xCE1 is set to high, xOEZ is set to low for Read operation, xOEZ is set to high for Write operation
2. Output state (High, Low or High-impedance) is determined by previous cycle control signals
3. xIA: used Address for Write/Read operation of memory
4. xCR: Counter Register

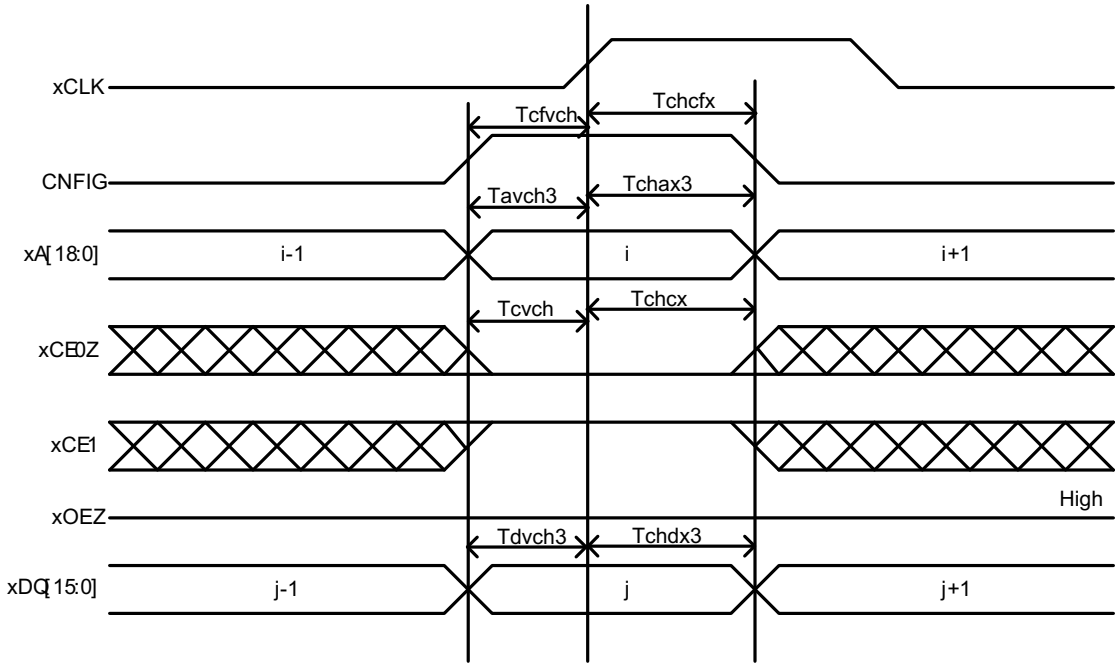
Timing Waveform 9: Scrub Operation for master mode (modes 1, 2)



Notes:

1. Scrub operation when ACE0Z = 0 or BCE0Z = 0 and CONFIG = 0, Enable EDAC and Enable scrub
2. xMBE is valid for flowthrough mode xCR: Counter Register
3. xMBE is invalid for pipeline mode
4. BUSYZ is kept high during slave mode operation

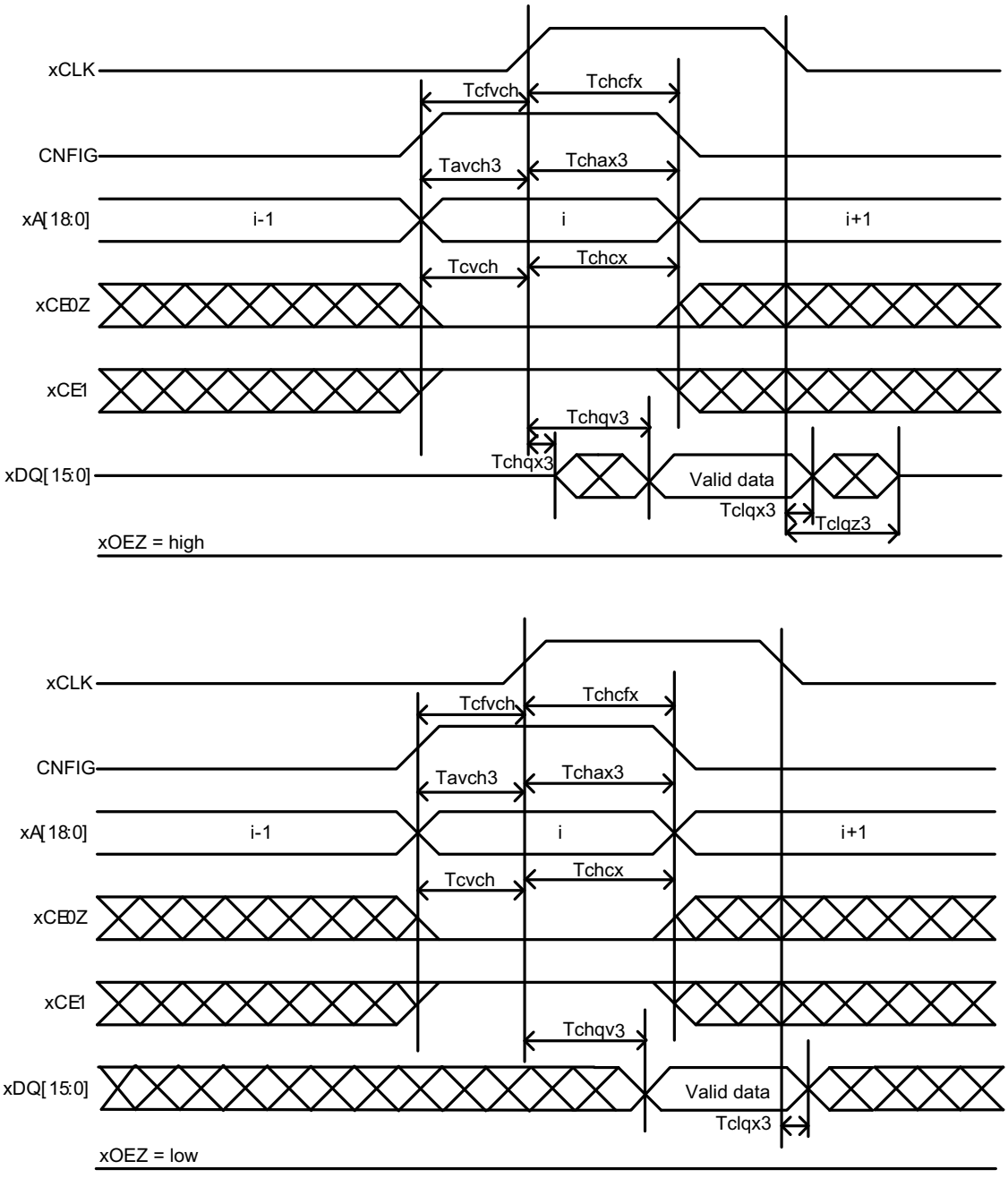
Timing Waveform 10: Configuration/Test Write mode



Notes:

1. ACE0Z is set to low; ACE1, AOEZ, CNFIG are set to high for writing into Control Register and Test Registers of Port-A
2. For Port-B test: BCE0Z is set to low; BCE1, BOEZ, CNFIG are set to high for writing into Test Registers of Port-B

Timing Waveform 11: Configuration/Test Read mode (mode 3)



Notes:

1. ACE0Z is set to low; ACE1, CNFIG are set to high for reading from Control Register and Test Registers of Port-A
2. For Port-B Test: BCE0Z is set to low; BCE1, CNFIG are set to high for reading from Test Registers of Port-B
3.

- **Test Modes (not recommended for customer/system use)**

This chip supports both SRAM test modes (clock mode, pull down control enable and margin tests) and EDAC test modes.

- Direct Mux Test: **stored data of the whole RAM** can be tested directly by disabling EDAC in the configuration mode (BER = 1) and controlling the PTE pin. When setting PTE to low, 16 data bits can be read out directly to 16 I/O pins on each port; if PTE is set to high, six parity bits will be read out to xDQ[5:0].
- Design for Test mode is done by strapping DFT pin to high. In this mode, the value of CKR register and PDR[3:0] registers must be configured after power up.
  - **Clock Mode**: This mode is controlled by CKR. When this register is set to high, internal self-time write circuit is disabled, the sense amplify latches data at the falling edge of xCLK
  - **Self-Time Control Test:** PDR{3:0} defines the timing margin for self-time circuit. In normal mode, the value 0110 of PDR[3:0] (13 pull down cells) gives ~150mV difference between BL and BLX for the sense amplify latching.
- Margin (stress) Test: There are four modes related to margin test for the RAM. These are controlled by STRESS[1:0]. The functions of these modes are briefly summarized as below:
  - "01" - normal mode: users use this mode in normal operation.
  - "00" - screen mode: speed up internally the timing. It is to detect weak or defective circuits.
  - "10" – slow mode: this mode is to add more delays to latch data output.
  - "11" – very slow mode: this is another yield mode to latch data output.
- A set of two registers is used to test the encoder, decoder of each ECC. All internal registers (Scrub Counter, Address Counters, Mirror Register and Control Register) can also be read out to test. The test is done separately for ECC of Port-A/Port-B. The CNFIG must be set to high to enter EDAC test modes. In test modes, memory access and scrub operation are inhibited.

- Test Write Register (6 bits) is used to test the encoder block. 16 data bits will be encoded to 6 parity bits and stored in this register for later reading out to test. In read phase, 6 parity bits from test write register and xMBE bit from test read register are read out on data bus x**DQ(6:0)**
- Test Read Register (16 decoded data bits + 1 error bit) is used to test the decoder block. 16 data bits and 6 lowest bits of address bus will be decoded and fixed error, then 16 decoded and fixed error data bits + 1 error bit xMBE stored in this register. In read phase, 16 data bits from test read register are read out on data bus x**DQ(15:0).**
  - Address Counters and Mirror Registers (19 bits) can be read out by its I/O port (16 bits) in two times. The setting is described in Table 9a/9b.
  - Scrub Counter (19 bits) can be read out by I/O (16 bits) of Port-A. in two times.

Table 9a: Test Mode Operation for Port-A

ACLK	AA7	AA8	AA9	AA10	Mode
/	X	L	L	L	Write Control Register
/	X	H	L	L	Read Control Register on ADQ(15:0)
/	X	L	H	L	Scrub Counter Out (16 lower bits) on ADQ(15:0)
/	X	H	H	L	Scrub Counter Out (3 higher bits) on ADQ(15:13)
/	L	L	L	H	ECC Write Block Test
/	H	L	L	H	ECC Write Block Register Out on ADQ(6:0)
/	L	H	L	H	ECC Read Block Test
/	H	H	L	H	ECC Read Block Register Out on ADQ(15:0)
/	L	L	H	H	Mirror Register Out (16 lowest bits) on ADQ(15:0)
/	H	L	H	H	Mirror Register Out (3 highest bits) on ADQ(15:13)
/	L	H	H	H	Counter Register Out (16 lowest bits) on ADQ(15:0)
/	H	H	H	H	Counter Register Out (3 highest bits) on ADQ(15:13)

Table 9b: Test Mode Operation for Port-B

BCLK	BA7	BA8	BA9	BA10	Mode
/	L	L	L	H	ECC Write Block Test
/	H	L	L	H	ECC Write Block Register Out on BDQ(6:0)
/	L	H	L	H	ECC Read Block Test
/	H	H	L	H	ECC Read Block Register Out on BDQ(15:0)
/	L	L	H	H	Mirror Register Out (16 lowest bits) on BDQ(15:0)
/	H	L	H	H	Mirror Register Out (3 highest bits) on BDQ(15:13)
/	L	H	H	H	Counter Register Out (16 lowest bits) on BDQ(15:0)
/	H	H	H	H	Counter Register Out (3 highest bits) on BDQ(15:13)

Table 10: Absolute Maximum Rating

Symbol	Parameter	Limits
V_{DD1}	DC supply voltage (Core)	-0.3 to 2.0V
V_{DD2}	DC supply voltage (I/O)	-0.3 to 3.6V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.6V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case	5°C/W
I_I	DC input current	±5 mA

Notes:

Stresses outside the listed absolute maximum ratings above may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond these rating conditions is not recommended. Exposure to maximum rating conditions for extended periods may affect the device's reliability and performance.

Table 11: Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD1}	DC supply voltage (Core)	1.35 to 1.65V
V_{DD2}	DC supply voltage (I/O)	3.15 to 3.45V
T_C	Case temperature range	(C) Screening: -55 to +150°C (W) Screening: -40 to +150°C
V_{IN}	DC input voltage	0V to V_{DD2}

Notes:

1. Measured for initial qualification. After process or design, changes could affect input/output capacitance.
2. Provided as a design limit but not guaranteed or tested.
3. Not more than one output maybe shorted at a time for maximum duration of one second.
4. $V_{IH} = V_{DD2}(max)$, $V_{IL} = 0$

Table 12: DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High-level input voltage		0.7*V_{DD2}		V
V_{IL}	Low-level input voltage			0.3*V_{DD2}	V
V_{OL}	Low-level output voltage	I_{OL}=4mA, V_{DD2}= V_{DD2}(min)		0.2*V_{DD2}	V
V_{OH}	High-level output voltage	I_{OH}=-4mA, V_{DD2}= V_{DD2}(min)	0.8*V_{DD2}		V
C_{IN}[1]	Input capacitance	*f* = 1MHz @ 0V		1.799	pF
C_{IO}[1]	Bidirectional I/O capacitance	*f* = 1MHz @ 0V		1.798	pF
I_{IN}	Input leakage current	V_{IN}=V_{DD2} and V_{SS}	-6	206	nA
`I_{OZ}	Tri-state output leakage current	V_O=V_{DD2} and V_{SS} V_{DD2}= V_{DD2}(max), GZ=V_{DD2}(max)	0	0	A
I_{OS}[2,3]	Short-circuit output current	V_{DD2}= V_{DD2}(max), V_O=V_{DD2} V_{DD2}= V_{DD2}(max), V_O=V_{SS}	-1	9	mA
I_{DD1}(OP_1)	V_{DD1} supply operating current @ 1MHz	Input: V_{IL}=V_{SS}+0.2V, V_{IH}=V_{DD2}-0.2V, I_{OUT}=0A V_{DD1}= V_{DD1}(max), V_{DD2}= V_{DD2}(max)		8	mA
I_{DD1}(OP_2)	V_{DD1} supply operating current @ 50MHz	Input: V_{IL}=V_{SS}+0.2V, V_{IH}=V_{DD2}-0.2V, I_{OUT}=0A V_{DD1}= V_{DD1}(max), V_{DD2}= V_{DD2}(max)		293	mA
I_{DD2}(OP_1)	V_{DD2} supply operating current @ 1MHz	Input: V_{IL}=V_{SS}+0.2V, V_{IH}=V_{DD2}-0.2V, I_{OUT}=0A V_{DD1}= V_{DD1}(max), V_{DD2}= V_{DD2}(max)		1	mA
I_{DD2}(OP_2)	V_{DD2} supply operating current @ 50MHz	Input: V_{IL}=V_{SS}+0.2V, V_{IH}=V_{DD2}-0.2V, I_{OUT}=0A V_{DD1}= V_{DD1}(max), V_{DD2}= V_{DD2}(max)		52	mA
I_{DD1}(SB)[4]	Supply stand-by current @ 0MHz	CMOS inputs, I_{OUT}=0A E1Z= V_{DD2}-0.2V, E2 = GND V_{DD1}= V_{DD1}(max), V_{DD2}= V_{DD2}(max)		5	mA
I_{DD2}(SB)[4]				5	uA
I_{DD1}(SB)[4]	Supply stand-by current @ 50MHz	CMOS inputs, I_{OUT}=0A E1Z= V_{DD2}-0.2V, E2 = GND V_{DD1}= V_{DD1}(max), V_{DD2}= V_{DD2}(max)		63	mA
I_{DD2}(SB)[4]				0.2	mA

Notes:

PTV: Strong_125_1.65V_3.6V
Stresses outside the listed absolute maximum ratings above may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond these rating conditions is not recommended. Exposure to maximum rating conditions for extended periods may affect the device's reliability and performance.

Table 13: Radiation Hardened Performance

Parameter	Description	Min	Typ	Max	Unit
TID	Total Ionizing Dose	300K	-	-	Rad (Si)
SER	Soft Error Rate (EDAC enabled)	<1e-10	-	-	errors / bit-day
LET	Linear Energy Transfer (latch-up immunity)	110	-	-	MeV-cm2

*Geosynchronous orbit solar min. with 100 mils of Al shielding

With EDAC enabled, the Scrub Engine should also be enabled and running at an appropriate frequency to prevent accumulation of errors in the memory in order to achieve consistently low SER over time.

Figure 3: Packaging Dimensions

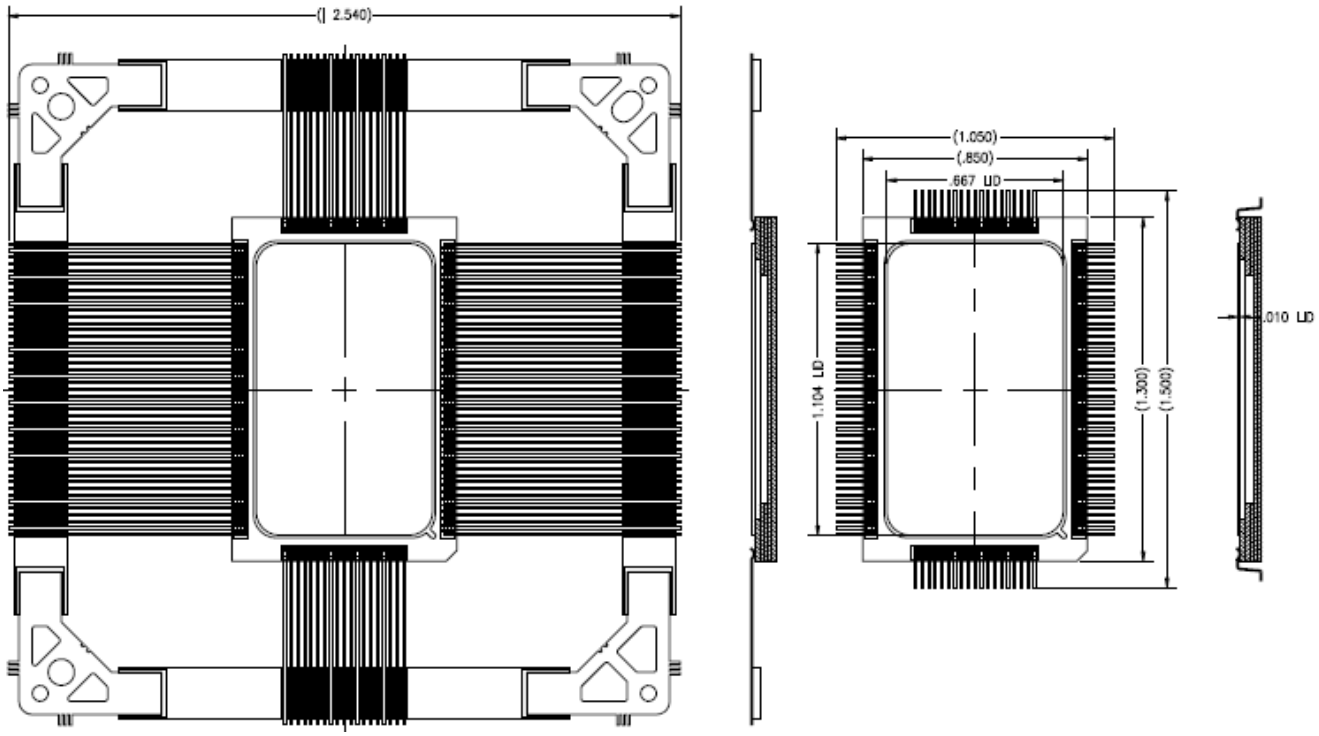


Table 14: Part Ordering Information

Description	Part number	Environment	Temperature Range	Package
High-temperature Synchronous Dual-port SRAM	HS512K16-CQ128A103E	Extreme temperature	-55° to 200°C	Ceramic 128 QFP
Radiation-hardened Synchronous Dual-port SRAM	HS512K16-CQ128A1F0E	Radiation-hardened	-55° to 125°C	Ceramic 128 QFP
High-temperature Synchronous Dual-port SRAM	HS512K16-DA103E	Extreme temperature	-55° to 200°C	Die
Radiation-hardened Synchronous Dual-port SRAM	HS512K16-DA1F0E	Radiation hardened	-55° to 125°C	Die

Table 15: Revision History

Revision Date	Changes	Author
March 30, 2010	Correct the read access time controlled by OEZ for timing waveform 1, 2 at the pages 13 , 14	SDS
May 14, 2010	Updated control register table with typical measured Scrub Rate and Scrub delay values by setting Reformatted AC Tables to place all modes side-by-side to simplify comparing modes Updated AC Tables with values extracted from characterization measurements Changed AC Timing Slew and Load footnote to reflect more reasonable load conditions Replaced Scrub Rate & Scrub Delay vs temperature tables with typical Scrub Rate and Scrub Delay % change vs Temperature graphs & typical temperature coefficients Added package drawing	SST
May 27, 2010	Updated control register table with typical measured Scrub rate and Scrub delay values by setting using nominal Vdd voltage instead of minimum Vdd voltage Updated typical Scrub Rate and Scrub Delay % change graphs to include fits at Vdd = Spec Low, Nominal and Spec High values	SST
Feb. 7, 2011	Updated clock to data valid (Tchqv) for pipeline modes to reflect larger sample testing results	SST
Feb. 17, 2011	Updated radiation performance numbers to reflect the actual results from radiation testing.	SST
Apr. 4, 2011	Added "Draft" watermark Added "SST Confidential" Footer Changed contact info to David Duff	SST
Nov 14, 2013	Radiation performance spec changed as follows TID > 300Krads SER < 1e-10 errors/bit-day (with ECC and Scrub) Dose rate up set threshold > 3e9 rads/sec (Si) Dose rate Survivability > 1e11 rads/sec (Si) SEL > 110 Mev (T=125C)	SST
Jan.1, 2014	Changed part number (remove CO35); removed watermark	SST
December 2015	Update to VORAGO format	
April 6, 2016 (Rev 1.1)	Added Radiation spec. Table 13 Added Part Ordering Information Table 14	VORAGO

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