



OBC ABACUS 2017



Description

ABACUS 2017 is an OBC unit with a general-purpose hardware platform, suited for a wide range of satellite missions.

It is designed to be flexible and scalable in terms of processing power, with the goal of maintaining a very low power consumption.

The presence of a MSP430 microcontroller and a Spartan-3E FPGA, organized in two independent but cooperative cores, provides the system with hardware redundancy and common mode fault tolerance.

The two cores offer many modalities to be implemented (e.g. Master/Slave or multi-Master) and the FPGA offers all the advantages of the RTL coding, for implementing specific tasks (e.g. attitude control) or generic systems also with IP cores of third parts.

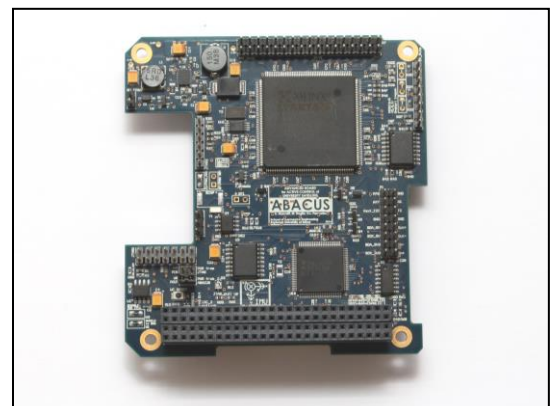
With the FPGA, high reliability may be achieved using TMR (triple modular redundancy) configuration codes.

Several embedded sensors provide health monitoring and attitude control data.

The system design offers the possibility to reconfigure the FPGA code and the MCU firmware in flight.

Primary Features

- Two cores (MCU MSP430 and FPGA Spartan-3E) directly interconnected with a 24 line bus;
- MSP430 EP series is a 16 bit RISC MCU running up to 25MHz. It is an HiRel Enhanced Product of Texas Instruments that supports Defense and Aerospace applications;
- 10 x 3,3V Analog Input and up to 45 x Digital GPIO channels;
- 16 x Voltage level shiftable GPIOs with interrupt features;
- 4 x COM ports (one of them also in RS422/485 standard levels Full or Half Duplex);
- 2 x I²C and 1 x SPI bus interfaces;
- Xilinx Spartan-3E FPGA RAM based core with 500K gates for intensive operations like ADCS, Image processing, or Turbo codes;
- 34 x GPIO (usable as LVDS) and 8 x GPI channels from FPGA;
- FPGA running at 25MHz or 100MHz (default);
- Embedded 16Mb (2MB) SRAM memory dedicated to the FPGA;
- FPGA and MCU reprogrammable from ground;
- Embedded IMU with 3 axis magnetometer, accelerometer and gyroscope;
- Embedded sensors: 3 x temperature sensors, 1 x drawn current monitor;
- Embedded RTC;
- Embedded 2 x 16MB flash NOR memories.





Other Features

- Both cores share the external sensors;
- Weight about 59 grams;
- PC/104 CubeSat form factor compatible;
- Several modalities for low power consumption (about 50mW with the FPGA OFF, the MCU ON and recording data from sensors on board);
- Powered from the 5V satellite bus;
- Off the shelf industrial grade / automotive components;
- Operating temperature range -40°C to +85°C.

Support

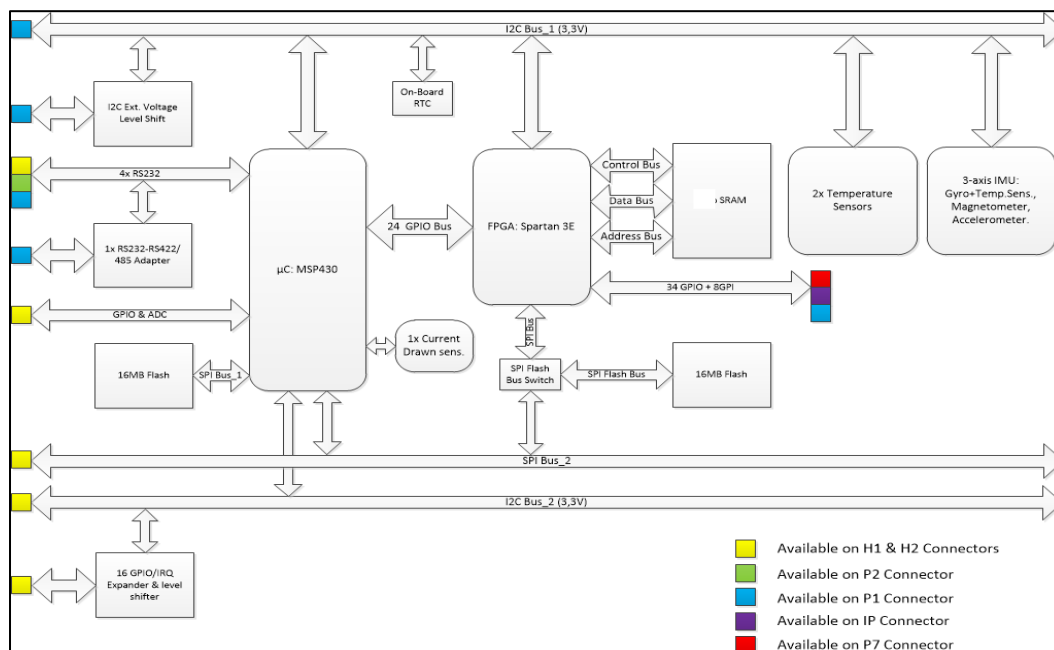
- User friendly software libraries are included: used on *UniSat-6*, *TigriSat* and *Serpens* satellites for the IMU, temperature sensors, RTC, flash memory, I2C, COM, SPI bus control and GPIO;
- Libraries are available for using ABACUS with GAUSS Radio and EPS, *AstroDev* radios and *GomSpace* EPS;
- A test example code for using the libraries is included.

Flight Heritage

ABACUS OBC flew on:

- UniCubeSat-GG (2012 , CubeSat 1U);
- UniSat-5 (2013, microsatellite of 32kg);
- UniSat-6 (2014, microsatellite of 26kg);
- TigriSat (2014, CubeSat 3U);
- Serpens (2015, CubeSat 3U).

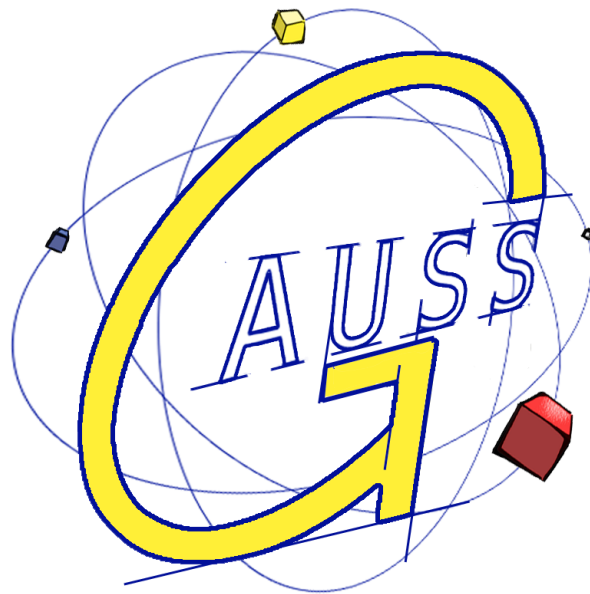
It will be one of the Onboard Computers in the next UniSat-7 mission (microsatellite 33kg):



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Datasheet

[ABACUS_201702]



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1. Introduction

ABACUS 2017 is an OBC unit with a general-purpose hardware platform, suited for a wide range of satellite missions. It is designed to be flexible and scalable in terms of processing power, with the goal of maintaining a very low power consumption. It is composed by two different cores, a MCU and a FPGA working cooperatively.

The MCU of ABACUS is a MSP430F5438A-EP manufactured by Ti (Texas Instruments). Ti already provides software examples in order to give the software developers examples on how to use the MCU. GAUSS Srl, however provides another set of libraries that helps the user to interface easily with all the components of the board requiring very little knowledge of the low level hardware involved.

You can use ABACUS Libraries as example code for developing your own software or you can also use directly these libraries on your code for easier development. Keep in mind that this software has already flown on some satellites like TigriSat, UniSat-6 and Serpens.

1.1. ABACUS Features

The presence of a MSP430 microcontroller and a Spartan-3E FPGA, organized in two independent but cooperative cores, provides the system with hardware redundancy and common mode fault tolerance.

The two cores offer many modalities to be implemented (e.g. Master/Slave or multi-Master) and the FPGA offers all the advantages of the RTL coding, for implementing specific tasks (e.g. attitude control) or generic systems also with IP cores of third parts.

With the FPGA, high reliability may be achieved using TMR (triple modular redundancy) configuration codes. Several embedded sensors provide health monitoring and attitude control data.

The system design offers the possibility to reconfigure the FPGA code and the MCU firmware in flight.

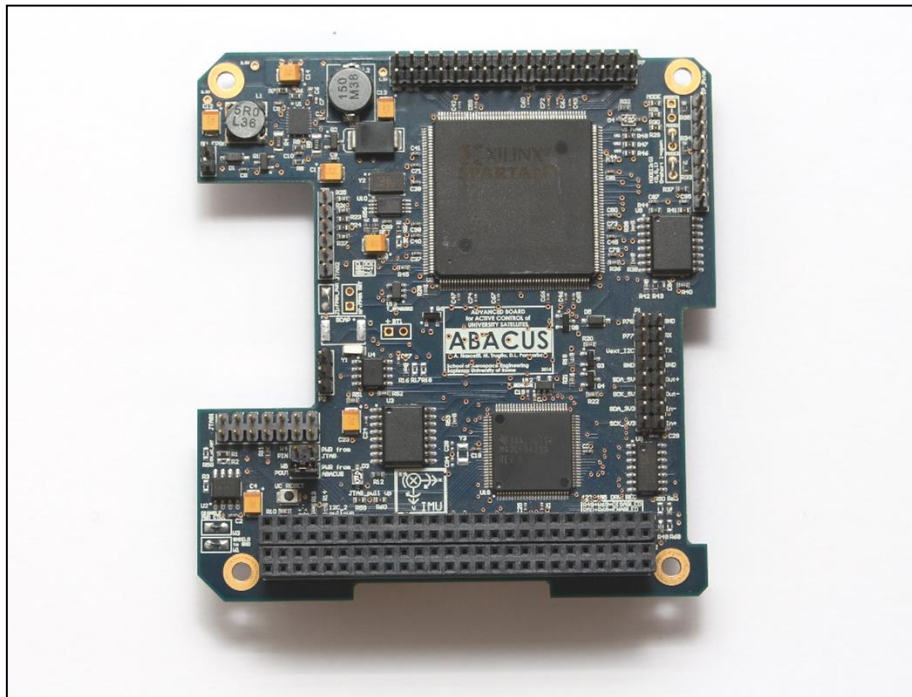


Figure 1 ABACUS OBC

The primary features of the board are:

- Two cores (MCU MSP430 and FPGA Spartan-3E) directly interconnected with a 24 line bus;
- MSP430 EP series is a 16 bit RISC MCU running up to 25MHz. It is an HiRel Enhanced Product of Texas Instruments that supports Defense and Aerospace applications;
- 10 x 3,3V Analog Input and up to 45 x Digital GPIO channels;
- 16 x Voltage level shiftable GPIOs with interrupt features;
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- Xilinx Spartan-3E FPGA RAM based core with 500K gates for intensive operations like ADCS, Image processing, or Turbo codes;
- 34 x GPIO (usable as LVDS) and 8 x GPI channels from FPGA;
- FPGA running at 25MHz or 100MHz (default);
- Embedded 16Mb (2MB) SRAM memory dedicated to the FPGA;
- FPGA and MCU reprogrammable from ground;
- Embedded IMU with 3 axis magnetometer, accelerometer and gyroscope;
- Embedded sensors: 3 x temperature sensors, 1 x drawn current monitor;
- Embedded RTC;



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- Embedded 2 x 16MB flash NOR memories.
- Both cores share the external sensors;
- PC/104 CubeSat form factor compatible ;
- Weight of 59 grams. (It might vary depending on your installed options);
- Several modalities for low power consumption (about 50mW with the FPGA OFF, the MCU ON and recording data from sensors on board);
- Powered from the 5V satellite bus;
- Off the shelf industrial grade / automotive components;
- Operating temperature range -40°C to +85°C.



1.2. Block Diagram

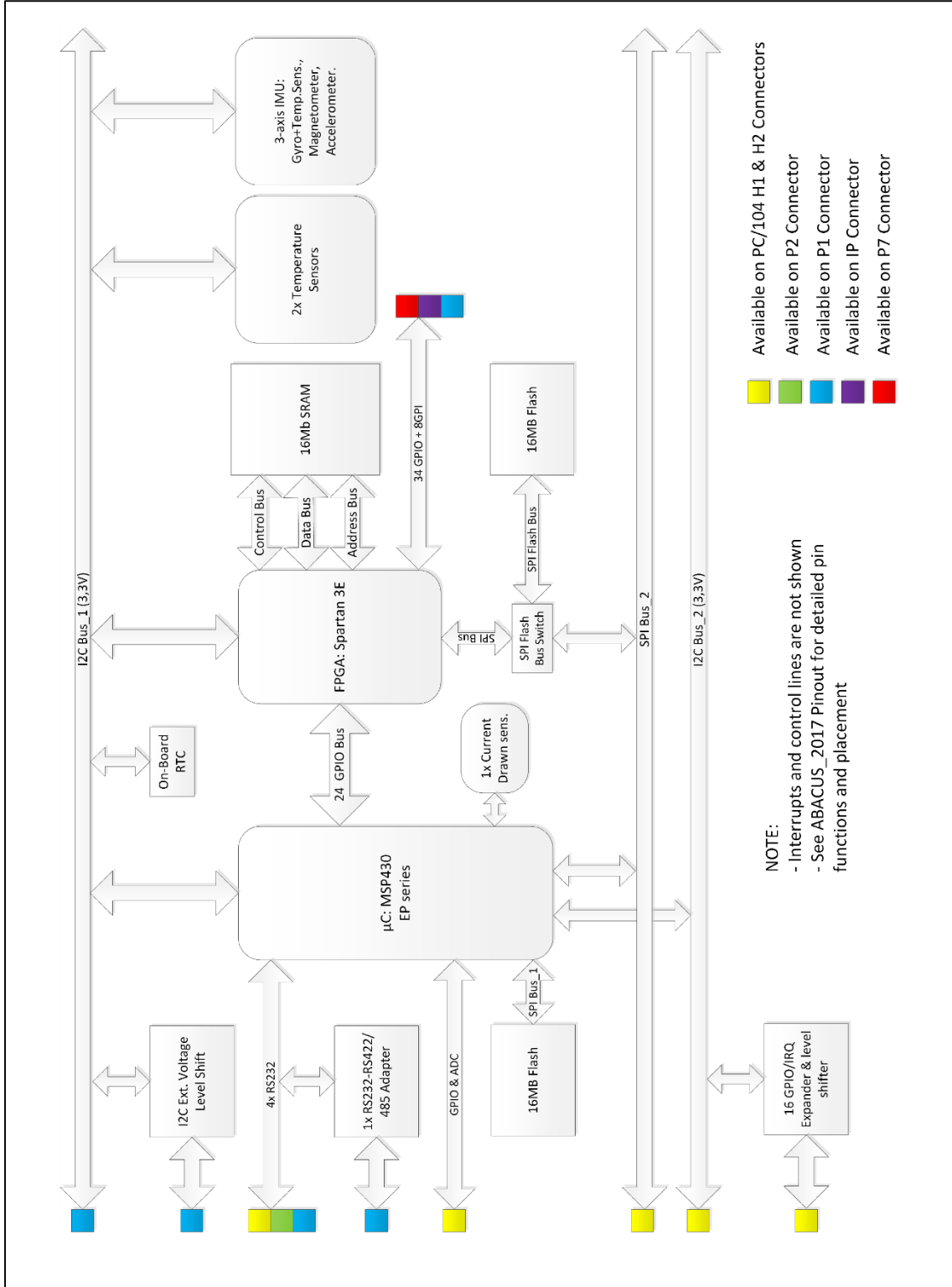


Figure 2 ABACUS General Overview



2. Pinouts

On this section the pinout of the ABACUS board is reported. All pins have a pitch of 2.54mm.

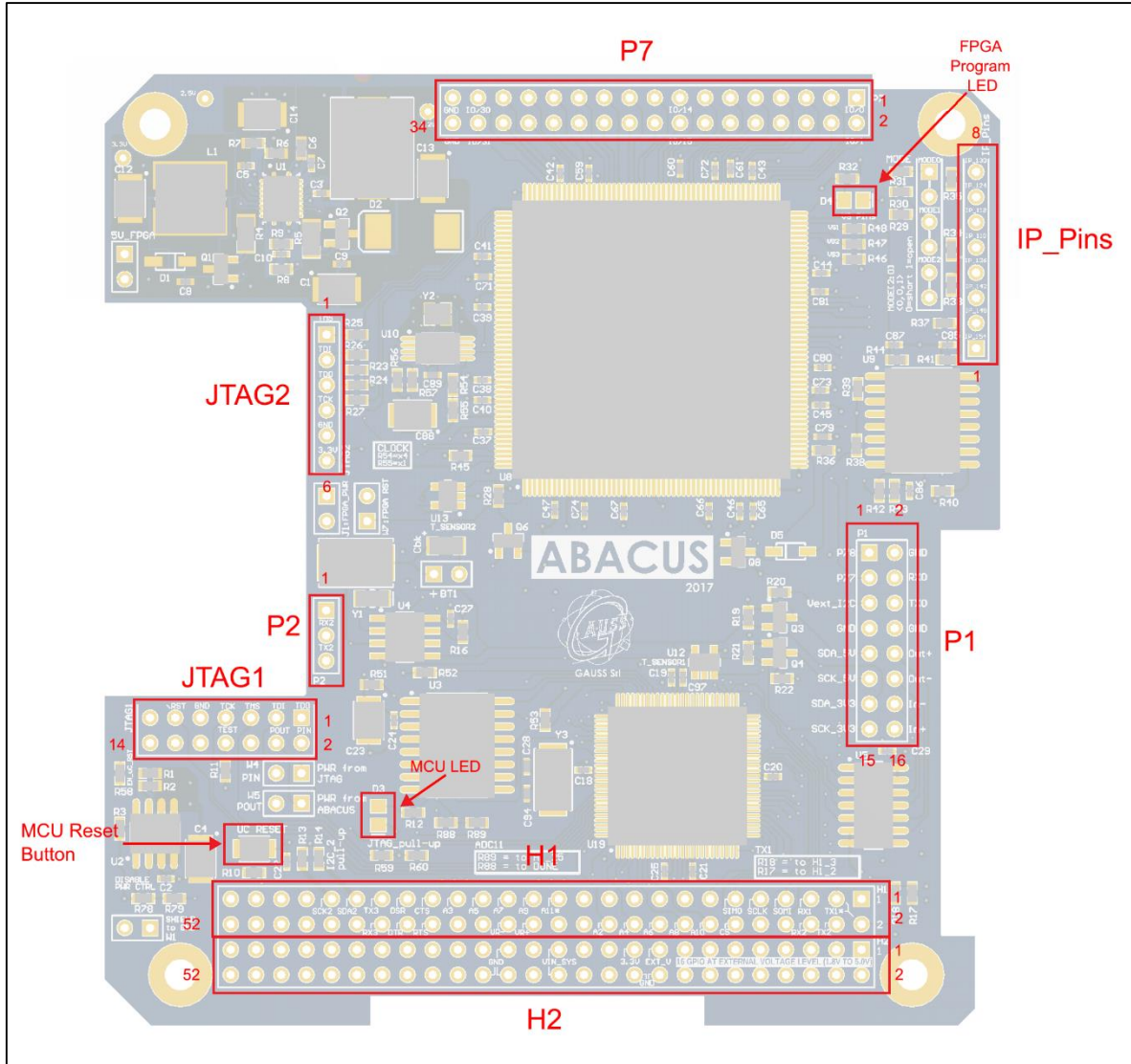


Figure 3 ABACUS Available ports



The following tables show the pinout of the different connectors on ABACUS. The colors of the following tables follow the color code reported on the block diagram on Figure 2.

PC104 pin	suggested config.	uC MSP430	PC104 pin	suggested config.	uC MSP430
H1_1	NC		H1_2	UART1_TXD/GPIO ***	P5.6 ***
H1_3	NC or UART1_TXD/GPIO ***	P5.6 ***	H1_4	UART2_TXD/GPIO *	P9.4 *
H1_5	UART1_RXD/GPIO	P5.7	H1_6	UART2_RXD/GPIO *	P9.5 *
H1_7	SPI_SOMI **	P5.4 **	H1_8	GPIO / RTC IRQ**	P2.0**
H1_9	SPI_SCK **	P5.5 **	H1_10	GPIO	P7.0
H1_11	SPI_SIMO **	P3.7 **	H1_12	SPI_CS/GPIO	P3.6
H1_13	GPIO	P2.2	H1_14	ADC10/GPIO	P7.6
H1_15	GPIO	P11.1	H1_16	ADC8/GPIO	P7.4
H1_17	NC		H1_18	ADC6/GPIO	P6.6
H1_19	GPIO	P10.0	H1_20	ADC4/GPIO	P6.4
H1_21	NC		H1_22	ADC2/GPIO	P6.2
H1_23	NC		H1_24	NC	
H1_25	NC or ADC11/GPIO ***	P7.7 ***	H1_26	NC	NC
H1_27	ADC9/GPIO	P7.5	H1_28	VREF+/VREF-/GPIO	P5.0
H1_29	ADC7/GPIO	P6.7	H1_30	VREF-/GPIO	P5.1
H1_31	ADC5/GPIO	P6.5	H1_32	NC	
H1_33	ADC3/GPIO	P6.3	H1_34	GPIO	P11.2
H1_35	CTS/GPIO	P3.3	H1_36	RTS/GPIO	P2.7
H1_37	DSR/GPIO	P3.0	H1_38	DTR/GPIO	P2.6
H1_39	UART3_TXD/GPIO	P10.4	H1_40	UART3_RXD/GPIO	P10.5
H1_41	I2C_SDA2 3.3V *	P10.1 *	H1_42	NC	
H1_43	I2C_SCK2 3.3V *	P10.2 *	H1_44	NC	
H1_45	NC		H1_46	NC	
H1_47	NC		H1_48	NC	
H1_49	NC		H1_50	NC	
H1_51	NC		H1_52	NC	

(*) Have to be used as I2C port, see Options Sheet for I2C pull-up resistors.
 (***) Have to be used as SPI port.
 (***) see Options Sheet.
 NB Changed from Abacus 2014

(**) same connection are also reported on external P2-CONNECTOR, UART2_RXD pin 1, UART2_TXD pin 2, GND pin 3
 (***) The pin H1_8 and P2.0 are always tied together and them can be connected also to the IRQ output of the RTC on-board. See Options Sheet
 (***) see Options Sheet.
 NB Changed from Abacus 2014

Table 1 ABACUS Connector H1 pinout

PC104 pin	fixed conf.	PC104 pin	fixed conf.
H2_1	GPIO EXP1 *	H2_2	GPIO EXP0 *
H2_3	GPIO EXP3 *	H2_4	GPIO EXP2 *
H2_5	GPIO EXP5 *	H2_6	GPIO EXP4 *
H2_7	GPIO EXP7 *	H2_8	GPIO EXP6 *
H2_9	GPIO EXP9 *	H2_10	GPIO EXP8 *
H2_11	GPIO EXP11 *	H2_12	GPIO EXP10 *
H2_13	GPIO EXP13 *	H2_14	GPIO EXP12 *
H2_15	GPIO EXP15 *	H2_16	GPIO EXP14 *
H2_17	GPIO EXP PWR IN **	H2_18	GND
H2_19	3.3V REG PWR OUT	H2_20	GND
H2_21	NC	H2_22	NC
H2_23	NC	H2_24	NC
H2_25	VIN_SYS (+5V)	H2_26	VIN_SYS (+5V)
H2_27	NC	H2_28	NC
H2_29	GND	H2_30	GND
H2_31	NC	H2_32	GND
H2_33	NC	H2_34	NC
H2_35	NC	H2_36	NC
H2_37	NC	H2_38	NC
H2_39	NC	H2_40	NC
H2_41	NC	H2_42	NC
H2_43	NC	H2_44	NC
H2_45	NC	H2_46	NC
H2_47	NC	H2_48	NC
H2_49	NC	H2_50	NC
H2_51	NC	H2_52	NC

(*) I2C to 16 GPIO expander
 (***) external source of pwr (1,8V - 5V) for GPIO EXP pins (optional or NC). See Selectable Options.

Table 2 ABACUS Connector H2 pinout



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P1 conn.	fixed conf.	NOTE	P2 conn.	fixed conf.
1	is connected to FPGA	FPGA pin 78	1	UART2_RXD/GPIO
2	GND		2	UART2_TXD/GPIO
3	is connected to FPGA	FPGA pin 77	3	GND
4	UART0_RXD *	uC P3.5		
5	I2C_1 pwr shift input		P7 conn.	FPGA Spartan3E pin
6	UART0_TXD *	uC P3.4	P7_1	106
7	GND		P7_2	107
8	GND		P7_3	108
9	I2C_SDA1 pwr shifted		P7_4	109
10	RS422/485 OUT+ *		P7_5	112
11	I2C_SCK1 pwr shifted		P7_6	113
12	RS422/485 OUT- *		P7_7	115
13	I2C_SDA1_3.3V **	uC P3.1 **	P7_8	116
14	RS422/485 IN- *		P7_9	119
15	I2C_SCK1_3.3V **	uC P3.2 **	P7_10	120
16	RS422/485 IN+ *		P7_11	122
	* An UART0 RS232 to RS422/485 adapter is used, UART0 and RS422/485 ports cannot be used together. See Selectable Options.		P7_12	123
	** Have to be used as I2C port		P7_13	126
			P7_14	127
			P7_15	128
			P7_16	129
			P7_17	132
			P7_18	133
			P7_19	134
			P7_20	135
			P7_21	137
			P7_22	138
			P7_23	139
			P7_24	140
			P7_25	144
			P7_26	145
			P7_27	146
			P7_28	147
			P7_29	150
			P7_30	151
			P7_31	152
			P7_32	153
			P7_33	GND
			P7_34	GND
JTAG1	uC MSP430 programmer		IP_Pins conn.	FPGA Spartan3E pin
1	JTAG TDO		IP_1 *	154
2	NC		IP_2 *	148
3	JTAG TDI		IP_3 *	142
4	3.3V		IP_4 *	136
5	JTAG TMS		IP_5 *	110
6	NC		IP_6 *	118
7	JTAG TCK		IP_7 *	124
8	JTAG TEST/SBWTCK		IP_8 *	130
9	GND			
10	NC			
11	JTAG Reset			
12	NC			
13	NC			
14	NC			
JTAG2	FPGA Spartan3E programmer			
1	TMS			
2	TDI			
3	TDO			
4	TCK			
5	GND			
6	3.3V			

* IP is an only input connector

Table 3 ABACUS Connectors P1, P2, P7, JTAG1, JTAG2 and IP_Pins pinout



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3. Inertial Measurement Unit Details

ABACUS comes with a 9DoF IMU:

- 3 Axis magnetometer
- 3 Axis gyroscope
- 3 Axis accelerometer

	Resolution	Sensitivity	Minimum Range	Maximum Range
Accelerometer	16 bit	0.0000610g LSB	2g	16g
Gyroscope	16 bit	0.0076(°/s) LSB	250 °/s	2000 °/s
Magnetometer	16 bit	0.15uT LSB		4800uT

Table 4 ABACUS IMU specifications

3.1. Orientation of Axes

The IMU is located on the bottom of the PCB (mounted upside down).

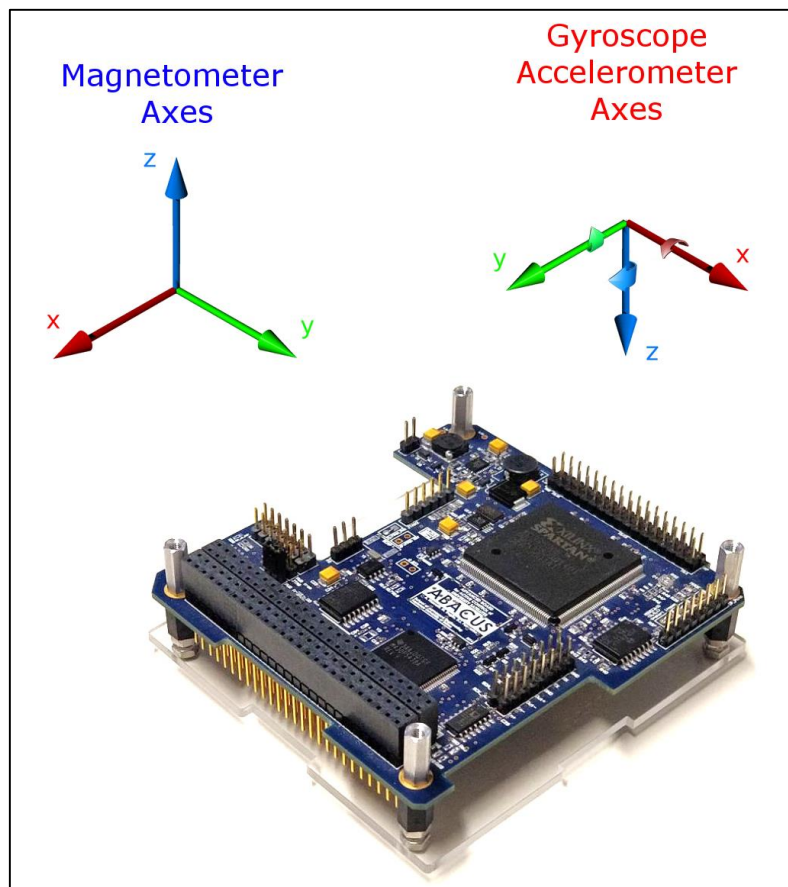


Figure 4 ABACUS IMU Orientation of Axes



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4. Absolute Maximum Ratings

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter *	Min	Max	Unit
Power Vcc pin (on H2 connector)	-0.3	+7	V
MSP430 IO pins (with I2C and SPI Bus)	-0.3	+3.6	V
FPGA IO pins (driver in Hi Z)	-0.85	+4.3	V
IO Expander pins (on H2 connector)	-0.5	+6.5	V
IO Expander IO-Power shift pin (H2_17)	-0.5	+6.5	V
RS422/485 Driver Out – Receiv. In volt.	-7.5	+12.5	V
I2C IO-Power shift pin (P1_5)	-0.3	+6	V
Storage temperature range	-55	+105	$^\circ\text{C}$

Table 5 ABACUS Absolute Maximum Ratings

* Voltages refer to GND

5. General Recommended Operating Conditions

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter *	Min	Typ	Max	Unit
Power Vcc pin (on H2 connector)	-	+5	+6.5	V
MSP430 IO pins (with I2C and SPI Bus)	-	+3.3	-	V
FPGA IO pins (driver in Hi Z)	-	+3.3	-	V
IO Expander pins (on H2 connector)	-	-	5.5	V
IO Expander IO-Power shift pin (H2_17)	+1.65	-	5.5	V
RS422/485 common mode voltage Vcm	-7	-	+12	V
I2C IO-Power shift pin (P1_5)	+3.3	-	+5	V
Temperature range	-40	-	+85	$^\circ\text{C}$

Table 6 ABACUS Recommended Operating Conditions

* Voltages refer to GND



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6. Electrical Characteristics

Considering $V_{cc} = 5V$. $T_A = 25^\circ C$, unless otherwise noted.

Parameter	Condition	Peak	Unit
Current	FPGA Off, MCU in sleep	10	mA
	FPGA Off, MCU at 1MHz	11	mA
	FPGA Off, MCU at 25MHz	16	mA
	FPGA at 25MHz, MCU at 25MHz*	90	mA
	FPGA at 100MHz, MCU at 25MHz*	130	mA
	At power up	160	mA

Table 7 ABACUS Electrical Characteristics

* With the provided test program



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7. Physical Characteristics and Drawings

Measure	Value
Mass including all connectors	62g
External size including all connectors	90.14 x 95.86 x 23.24 mm

Table 8 ABACUS Physical Characteristics

All dimensions are in mm.

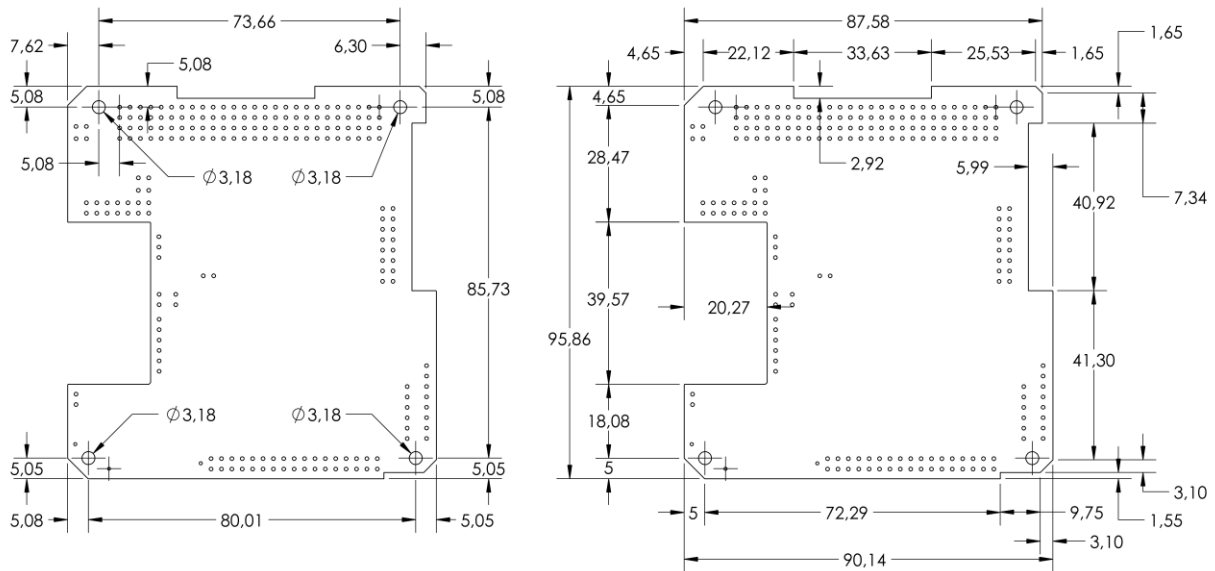


Figure 5 ABACUS Physical Dimensions TOP

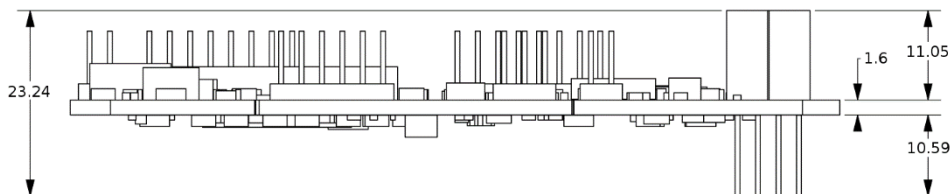


Figure 6 ABACUS Physical Dimensions side