

CHAMPS Flight Computer (MPSoC CFC-400)



28 VDC unit with XCVR ports
 (36 mm height)

Innoflight's Compact Hybrid Architecture for Multi-Parametric Sensing (CHAMPS) is a next-generation flight computer in Innoflight's Compact Flight Computer (CFC) family that is designed with a hybrid architecture to provide a mixture of:

- High-reliability operation based on rad-tolerant electronics parts, and
- High-performance operation based on the latest COTS technology

CHAMPS is provided with CubeSat-compatible SWaP, with an 82 mm x 82 mm enclosure and dynamically configurable performance with power ranging from ~0.6 W up to ~12 W. CHAMPS has many possible applications, including use as: a high-reliability C&DH processor; a high-performance payload data processor; a High-Assurance End Cryptographic Unit (ECU) with built-in cyber protection; or all of the above in one unit. CHAMPS supports many software environments and is provided with a rich middleware infrastructure to facilitate coordination between the high-reliability and high-performance sections of the architecture.

Specification	Value	Comment
Supply Voltage	Two options: 1) Unregulated 28 VDC 2) Regulated 3.3 VDC	The 28VDC option includes an isolated, rad-tolerant DC/DC converter
Power	0.6W to 12W	CHAMPS can adjust its performance and power dynamically as needed by the mission CONOPS
Operating Temperature	-40° to +85° C	Temperature limits at the mounting interface
Random Vibration Level	NASA GEVS	Conforms to NASA General Environmental Verification Standard, GSFC-STD-7000
Operating Pressure	Hard vacuum	--
Dimensions	(82 X 82 X 29) mm	No daughter card, regulated 3.3 VDC and no XCVR ports. Includes enclosure designed for EMI and Thermal
Mass	≤ 250 gram	Includes full enclosure
Radiation Tolerance	30 krad TID; SEL immune	Designed for tactical space missions
High-Reliability Platform	<ul style="list-style-type: none"> • MicroSemi Rad-Tolerant FPGA with <ul style="list-style-type: none"> ○ LEON3FT CPU • 8 MB MRAM 	The MRAM is shared between the high-reliability and high-performance platforms. Engineering Model includes non-RT parts. Flight Model available with non-RT parts option.
High-Performance Platform	<ul style="list-style-type: none"> • Xilinx MPSoC device with <ul style="list-style-type: none"> ○ ARM Cortex-A53 quad-core APU @ up to 1 GHz ○ ARM Cortex-R5F dual-core lockstep RPU @ up to 600 MHz ○ FPGA fabric: ~275k LUTs, ~550k flip-flops, ~4 MB block RAM • Volatile (CPUs): 2 GB ECC-protected LPDDR4 • Volatile (FPGA): 256 MB DDR3 • Non-volatile <ul style="list-style-type: none"> ○ 16 GB SLC NAND flash ○ 8 MB MRAM 	Offered with 3 standard development environments: <ul style="list-style-type: none"> • Pre-configured hardware: PL bitstream with high-speed peripheral interfaces; Xen Dom0 (system control domain) with hardware drivers; Xen DomU (user domain) build environment with virtualized interfaces • Same as above plus Xilinx SDSoC support: Innoflight provides the SDSoC platform; the user can apply remaining FPGA resources to code acceleration • Option 3: Just BSP + drivers: for users that are FPGA capable and want to develop their own fully-custom bitstreams
I/O	<ul style="list-style-type: none"> • Low speed: serial (up to 4 ports), SPI / I2C (up to 2 ports each), MIL-STD-1553 (dual redundant), analog (4 inputs, 1 output) • Medium speed: 44 configurable pins • High speed: configurable high-speed serial lanes (x2 on Processor Board and x8 additional on optional daughter card, including two-lane Gen2 PCI-Express) 	<ul style="list-style-type: none"> • Serial ports can be configured for different combinations of 3.3V versus RS-422 physical layer and UART versus sync serial link layer • Medium-speed example: 20 LVDS pairs (up to 700 Mbps each with SERDES) • High-speed serial lanes can operate up to 16 Gbps each and support protocols such as SGMII, SRIO, PCI-Express, Aurora, and more