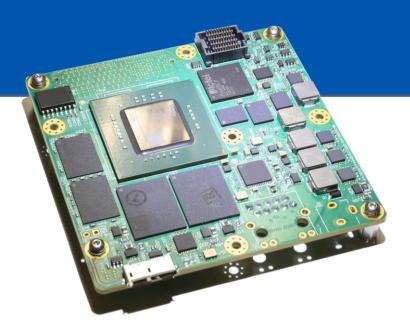
Q8 SPECIFICATIONS





FEATURE HIGHLIGHTS

Industry-Leading Performance The Q8 features a Multi-Processor System-on-Chip (MPSoC), including multi-core CPUs providing 64-bit processor scalability supported by massive programmable logic resources and a wide array of hardware interfaces.

Low Mass, Volume, Power The Q8 measures 80 mm x 80 mm x 11.2 mm and consumes as low as 4 W. Its small size, low mass and power consumption make the Q8 ideal for aerospace applications that demand extremely high performance.

Integrated Hybrid Environment The application space in a Q8 is a tight integration of a quad-core ARM Cortex-A53 Application Processing Unit, a dual-core ARM Cortex-R5 Real-Time Processing Unit, an ARM Mali-400 GPU and programmable logic, featuring 504,000 system logic cells, 461,000 flip-flops, 274,000 lookup tables and 1,728 DSP slices reserved for application-specific use.

Flexible Interfacing

Applications

The Q8 provides Gigabit Ethernet networking through its RJ45 connector along with USB 2.0 & USB 3.1 Gen 1 host ports. The Q8 also provides multiple digital I/O lines, including up to 52 GPIO, 12 MIO, 64 LVDS pairs, 3 Gigabit transceivers, USB 2.0 and factory-selectable RS-232/422/485 through its mezzanine connector.

The extremely high performance and extensive FPGA fabric make the Q8 ideally suited for onboard:

- Synthetic Aperture Radar (SAR) processing
- Hyper/multispectral compression
- Stereo and monocular visual odometry
- Image registration and alignment
- Convolutional neural networks
- · Advanced Software Defined Radios (SDR)

OVERVIEW

The Q8 is the highest performance member of the Xiphos Q-Card family of low-cost, embedded nodes for control, processing and interface applications, primarily for aerospace markets. Q-Cards combine a small form factor with broad networking, processing and I/O capabilities.

At the core of each Q8 is a hybrid environment of powerful multi-core CPUs and reprogrammable logic, providing consistent and reliable performance. The library of logic and software functions is augmented by onboard digital I/O.

FLIGHT HERITAGE

The Q8 is the latest in the line of space qualified Q-Cards. The first flight of the Q8 is planned for Q3 2019. The Q8's predecessors include the Q7, Q6, Q5 and Q4:

- The Q7's space version, Q7S, has been operating in orbit since June 2016. The Q7S is certified for manned space flight and is used on the International Space Station (ISS).
- The Q6 was first flown in August 2011, with almost 100 units delivered to customers worldwide. It was also certified for manned space flight and used on the ISS.
- The Q5 was first flown in June 2004.
- The Q4 was first flown in December 2002 and was also certified for manned space flight and used on the ISS.





Front & Back





Product Integration Module (PIM)

Each Q8 is delivered with a detachable PIM to facilitate development. The PIM provides standard commercial interfaces (e.g. CAN, 1-wire, 4 RSXXX, JTAG, 13 digital I/O, 8 analog input, 4 analog output), debug LEDs and other lab development features.

Software Development

Xiphos provides an Application Development Kit with standard Linux libraries for C/C++ to support software development on Linux workstations. *Code previously developed for Linux desktop and server applications can be easily ported to the Q8.* Q8 hardware and logic interfaces are all accessible through either standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

Logic Development

Logic development uses standard Xilinx development tools. Xiphos, Xilinx and many third-party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.



Characteristics (Rev B Board)

Memory

- 4 GB LPDDR4 DRAM
- 2x 128 MB QSPI Flash (NOR)
- 2x eMMC, 128 GB each, on independent buses / power control

Multi-Processor System-on-Chip

- Xilinx Zyng UltraScale+ XCZU7EG
- Quad-core ARM Cortex-A53 Application Processing Unit at up to 1.2 GHz
- Dual-core ARM Cortex-R5 Real-Time Processing Unit at up to 500 MHz
- · ARM Mali-400 GPU at up to 600 MHz
- 504,000 system logic cells
- 461,000 flip-flops (FF)
- 274,000 lookup tables (LUT)
- 1,728 DSP slices

Control FPGA

Microsemi ProASIC3

Operating System

- Linux 4.14 LTS
- Robot Operating System (ROS)

Real Time Clock

- RTC with sleep & wake-up on alarm/interrupt
- Dedicated power pin for external battery

Power

- 4 W 25 W, scalable
- 6 to 16 VDC
- Various power modes (including deep sleep)
- Overcurrent detection & protection (global and local) and brownout protection

Form Factor

- 85.8 mm x 80 mm x 22.6 mm (with RJ45 and power connectors)
- 80 mm x 80 mm x 11.2 mm (without connectors)

Environmental

• Operating Temperature -40 to +60°C

Interfaces

- Power
- Gigabit Ethernet (RJ45)
- USB 2.0 & USB 3.1 Gen 1 hosts (USB Type C)
- CAN Bus controller
- Up to 38 single-ended GPIO 3.3 V, 14 single-ended GPIO 1.8 V, 12 MIO 1.8 V, 64 LVDS pairs/128 single-ended GPIO 1.8 V, 3 Gigabit transceivers (SATA, PCI express), USB 2.0 and factory-selectable RS-232/422/485 (Mezzanine connector)

Space-Qualified Features (Q8S)

- Triple-mode redundancy (ProASIC3)
- EDAC-protected RAM
- Upset and multi-current monitoring
- FPGA bit-stream scrubbing
- Software robustness / watchdog, etc.

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