HyperScape100

Datasheet

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Document History

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1	2019-10-07	First Release
2	2019-10-10	Updated mechanical drawings

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List of Abbreviations

Abbreviation	Description
A	Ampère
ADC	Analog to Digital Converter
BOL	Beginning of Life
°C	Degree Celsius
CAN	Controller Area Network
CCD	Charge Coupled Device
CE	Control Electronics
CMOS	Complementary Metal Oxide Semiconductor
CSKB	CubeSat Kit Bus
DC	Direct Current
FPGA	Field Programmable Gate Array
FEE	Front-End Electronics
FWHM	Full Width at Half Maximum
GND	Ground
g_{rms}	Gravitation Constant, Root Mean Square (g = 9.81 m/s^2)
GPIO	General Purpose Input Output
GSD	Ground Sampling Distance
HPP	Half Power Point
Hz	Hertz
I^2C	Inter-Integrated Circuit
I/O	Input / Output
kg	Kilogram
kHz	Kilohertz
km	Kilometre
krad	Kilorad
LEO	Low Earth Orbit
lp	Line Pairs
LVDS	Low Voltage Differential Signalling
mA	Milliampere
MHz	Megahertz
mm	Millimetre
ms	Milliseconds
nm	Nanometre
OFE	Optical Front-End
PCB	Printed Circuit Board
SDR	Single Data Rate
SEL	Single Event Latch-up
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SU	Sensor Unit

Abbreviation	Description
TDI	Time Delay Integration
TID	Total Ionising Dose
U	Unit (CubeSat)
µm	Micrometre
V	Volt
VNIR	Visible and Near-Infrared
W	Watt

1. Overview

The HyperScape100 is a hyperspectral push-broom imager primarily designed for earth observation applications as a payload for CubeSat satellites. It is based on 12.6-megapixel image sensor and continuously variable filter in the visible and near-infrared (VNIR) spectral range. The HyperScape100 provides continuous line-scan imaging in up to 32 spectral bands, each with digital time delay integration (TDI).

The optical front-end (OFE) has a large aperture diameter and long focal length within a compact form factor, resulting in a ground sampling distance (GSD) of 4.75 m at an orbital height of 500 km. The modified Cassegrain optical design brings performance to the edge of the object field over the whole spectral range at an ultra-low distortion. The HyperScape100 is engineered to withstand the rigours of the space environment and maintain performance across a wide temperature range. Its compact form factor is optimised for integration into 3U or larger CubeSat structures.

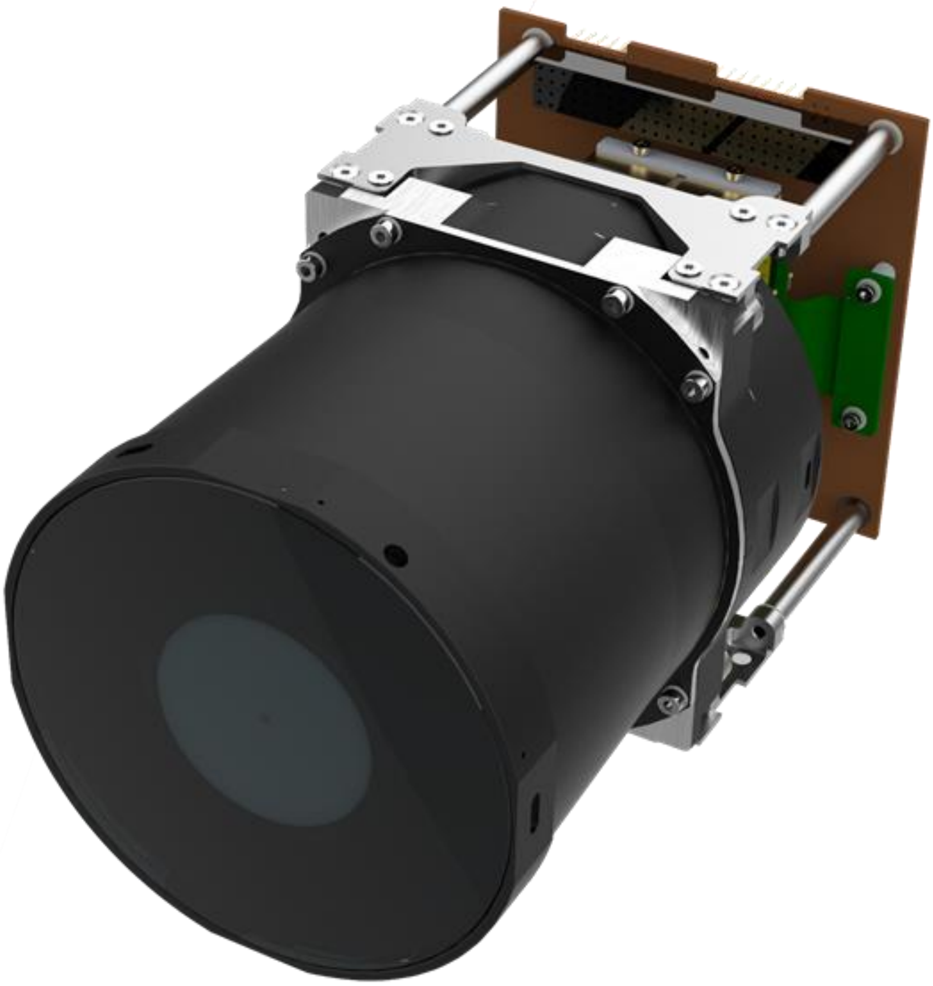

Figure 1-1: HyperScape100 Imager

1.1 Features

- 4.75 m GSD (at 500 km orbit height)
- The swath of 19.4 km (at 500 km orbit height)
- Up to 32 spectral bands in the VNIR range
- FWHM bandwidth of 4% of the central wavelength
- 128 Gigabyte non-volatile storage capacity for up to 3900 km strip (at 500 km orbit height)
- On-board image processing and compression (optional)
- Comprehensive onboard telemetry and health monitoring
- Environmental verification based on GSFC-STD-7000

1.2 Applications

- Precision agriculture
- Forestry and land use
- Energy and infrastructure
- Coastal monitoring
- Air quality

1.3 Key Specifications

Table 1-1: Key Specifications

Optics	
Focal Length	580 mm ±1 mm
Aperture	95 mm
Full Field of View	2.22° (Across Track)
Imaging	
Configuration	Line-scan (push broom)
Sensor Technology	CMOS
Cross Track	4096 pixels
Pixel Size	5.5 µm
Pixel Depth	10-bit
Spectral Bands	Up to 32
TDI Stages	Up to 32 per band (user assigned)
Line Rate	Up to 2600 Hz (1)
Spectral Range	487 nm – 790 nm (filter option 1) 502 nm – 801 nm (filter option 2) 516 nm – 810 nm (filter option 3)
Spectral Band Width	FWHM: ~4% of the central wavelength
Transmittance	51% (at 550 nm) (2)
On-Board Electronics	
Storage Capacity	128 Gigabyte NAND Flash
Continuous Strip Length	Up to 800 km (3)
Image Processing	Binning, Thumbnails
Image Compression	Lossy/Lossless (optional)
Control Interface	I^2C or SPI CAN, RS-422 (optional) Customer specific interface (optional)
Data Interface	LVDS (or customer specific interface, optional)
Power Supply	5 V DC
Power Consumption	< 6 W (during imaging mode)
Mechanical	
Mass	1.2 kg
Dimensions	98 x 98 x 176 mm
Environmental	
Operating Temperature	-10 to +50 °C
Radiation (TID)	> 15 krad

(1) Dependant on orbit height, see Figure 3-1
(2) Including filter
(3) At 500 km orbit height

1.4 Functional Components

The HyperScape100 imager consists of the following functional components:

- **Optical Front-End (OFE)**: The xScape100 VNIR OFE is used to focus the incoming light onto the focal plane.
- **Sensor Unit (SU):** It consists of the CMOS sensor front-end electronics (FEE) and a continuously variable filter. It also includes the sensor plate mechanics which allows it to be mounted at the OFE's focal plane.
- **Control Electronics (CE)**: The CE provides control and data interfaces to the satellite bus. It performs sensor control, data handling, data storage, and image processing. It is also responsible for power regulation and management, as well as health monitoring and telemetry.

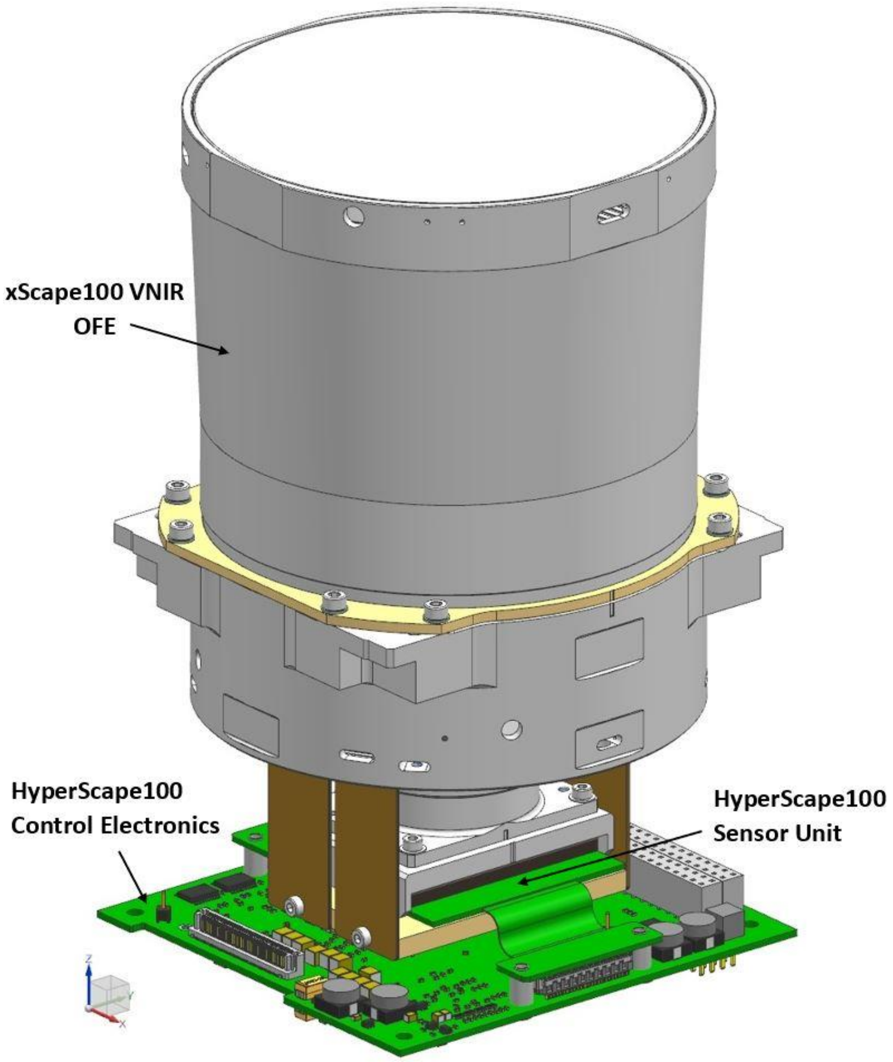

Figure 1-2: HyperScape100 Functional Components

2. Detailed Description – Optical Front-End

The xScape100 VNIR OFE is used as an optical front-end for the HyperScape100. Following the unique demands of space-based imaging payloads, the xScape100 VNIR OFE was designed to accommodate a wide spectral range, be robust and maintain performance across a wide temperature range. The optical design of the imaging payload incorporates a modified Cassegrain optical design with a meniscus entrance lens which defines the entrance pupil of the payload and adds additional environmental protection to the OFE during integration, launches and in operation.

Table 2-1: OFE Characteristics

Description	Value
Focal Length	580 mm ± 1 mm
F-Number	6.1
Front Aperture Diameter	95 mm
Obscuration Diameter	47.2 mm
Distortion	< 0.165%
On-Axis MTF	18% at Nyquist (93 lp/mm)

For further information, see the xScape100 VNIR OFE Datasheet.

3. Detailed Description – HyperScape100 Sensor Unit

The HyperScape100 Sensor Unit houses the Front-End Electronics (FEE) which is based on a 12.6-megapixel CMOS sensor. The sensor is fitted with a continuously variable filter, and three standard spectral range selections are available, as shown in Table 3-1. The out-of-band transmittance of the filter is less than 0.01%.

Table 3-1: Filter Range Options

Filter	Spectral Range
Option 1	487 nm – 790 nm
Option 2	502 nm – 801 nm
Option 3	516 nm – 810 nm

The windowing mode of the sensor allows the capturing of up to 32 user-selectable spectral bands. The bandwidth of each band is approximately 4% of the centre wavelength. This results in the FWHM increasing from 19.4 nm at 487 nm to 32.4 nm at 810 nm. The centre wavelength of each band can be selected in steps of 0.4 nm. The nature of the continuously variable filter means that the TDI stages applied to each band influence not only the signal-to-noise ratio (SNR) but also the bandwidth. Fortunately, the increase in bandwidth for a typical number of TDI stages is very small. Even with 16 TDI stages, the effective increase in bandwidth is less than 8%, as shown in table Table 3-2.

Table 3-2: Spectral Band Examples

Centre Wavelength (nm)	TDI Stages	FWHM Bandwidth (nm)	SNR
487	1	19.4	14.9
487	8	20.2	42.3
487	16	21.0	59.9
810	1	32.4	24.2
810	8	33.1	68.4
810	16	33.9	96.7

The number of TDI stages for each band may be individually selected by the user in multiples of 2, to a maximum of 32. The sum of all the TDI stages (across all the bands) is limited by the line scan rate, which is determined by the orbit height for earth observation satellites, as shown in Figure 3-1. The graph clearly shows that at lower orbit heights, an increased line scan rate reduces the total number of TDI stages available. For example, at 500 km orbit height, a total of 320 TDI stages are available so that the user may select 10 TDI stages for each of the 32 bands.

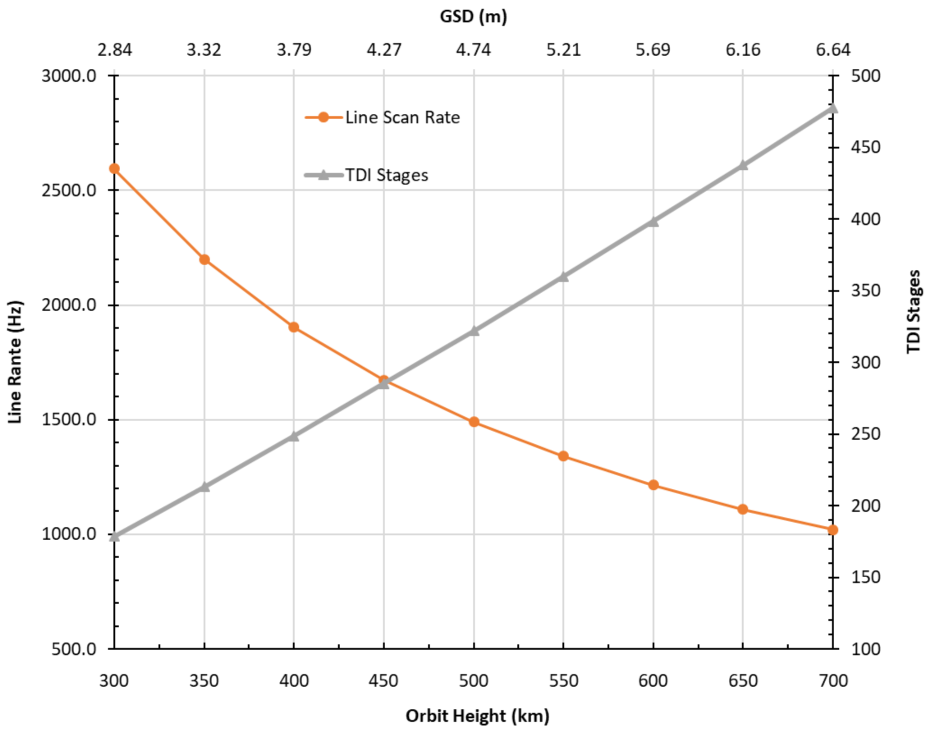

Figure 3-1: Line Rate and TDI Stages

The signal-to-noise ratio with a selection of TDI stages, at an orbit height of 500 km is shown in Figure 3-2. A radiance level of 100 W·m^{-2}·sr^{-1}·µm^{-1} is assumed across the spectral range for all of the SNR values.

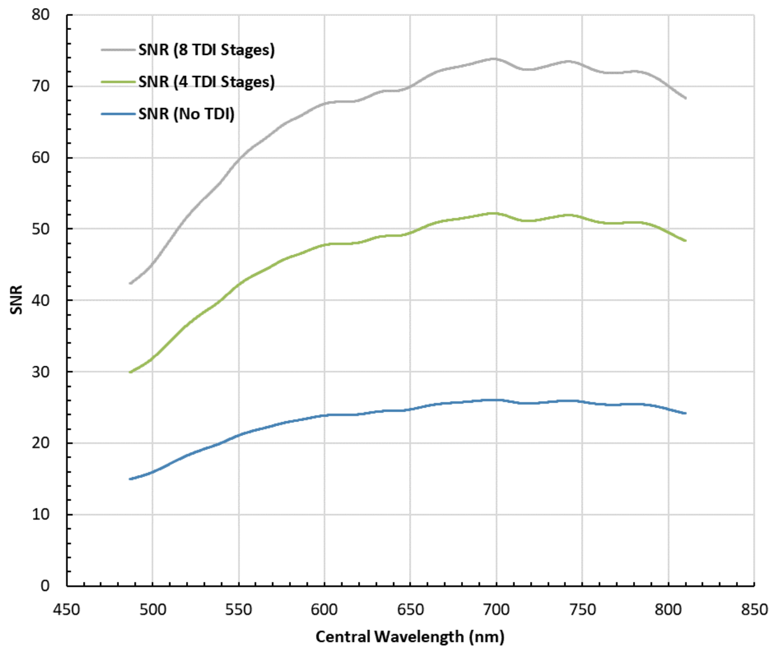

Figure 3-2: SNR vs Central Wavelength

4. Detailed Description – Control Electronics

The Control Electronics (CE) is a single PCB with a standard PC-104 form factor. It interfaces to the Front-End Electronics (FEE) of the HyperScape100 Sensor Unit as well as the external satellite bus. The functionality of the CE is largely based on a high-performance FPGA, which allows image data to be captured at high data rates, processed on-board, and delivered via a high-speed interface. The CE is highly configurable, with several standard selections and options available, which allows for flexible integration into existing systems.

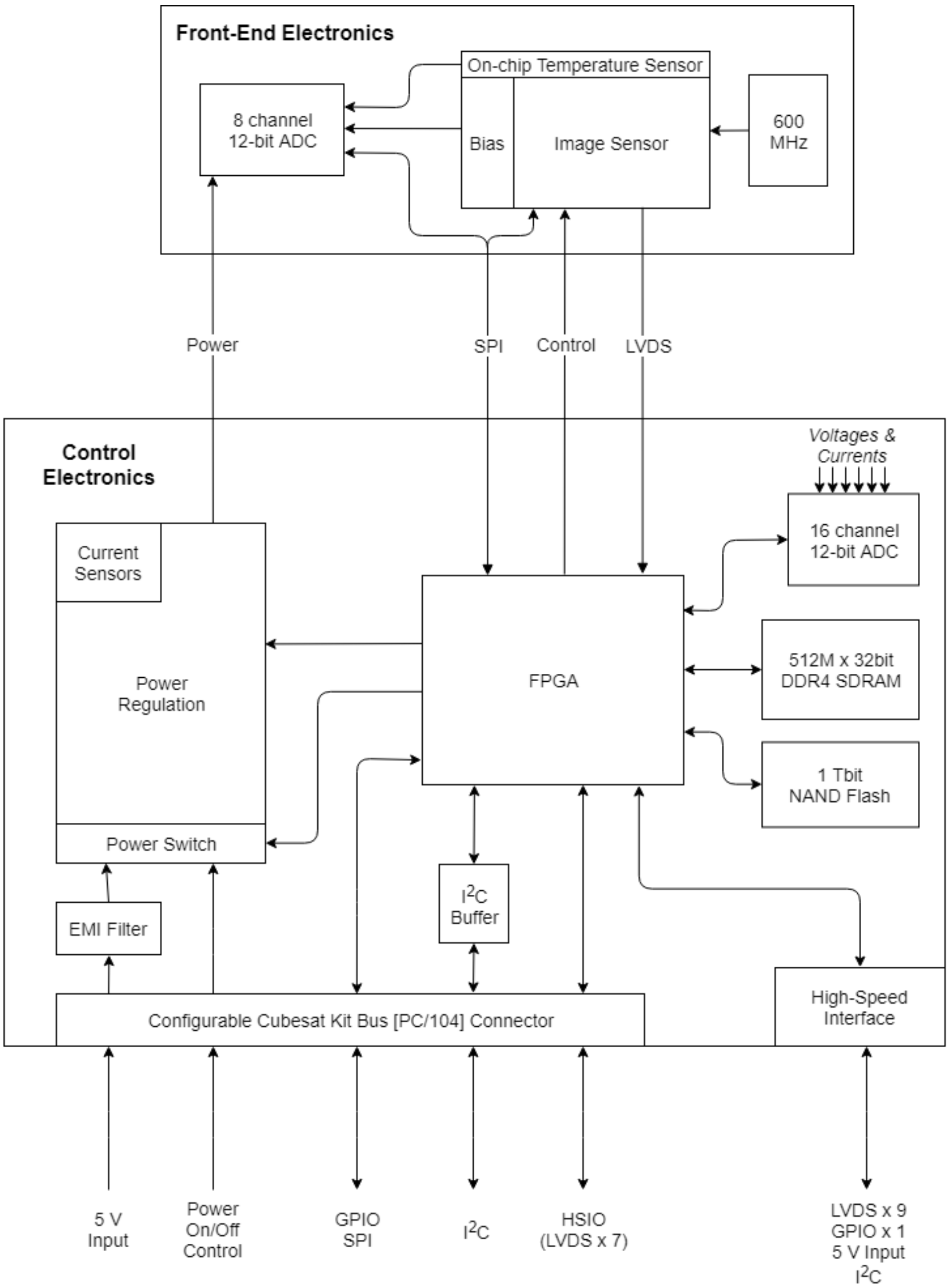

Figure 4-1: Control Electronics Block Diagram

4.1 Power Supply

The CE requires a direct current (DC) power supply regulated at 5 V ± 10% with a current rating of at least 1.5 A. Typically, the satellite bus supplies a switched power supply to the CE. In cases where the power supplied to the CE is not switched, user control of an on-board power switch is available. The CE monitors the current consumption of various sub-circuits and can initiate a full power-down or power-cycle if an over-current event occurs. This serves to protect against radiation-induced single-event latch-up (SEL). The different power switching possibilities are shown in Table 4-1

Table 4-1: Power Switching Alternatives

Power Mode	Description	Over-current
Bus Switched	External 5 V supply is switched.	Power-cycle
User-Controlled Switch (Direct)	External 5 V supply stays ON. Switch ON – Power Control line is driven high Switch OFF – Power Control line is driven low	Power-cycle
User-Controlled Switch (Latched)	External 5 V supply stays ON. Switch ON – Power Control line is driven high Switch OFF – Control command to CE	Power-cycle or Power-down (1)

(1) Drive the Power Control line low for over-current power-down, or high for power-cycle.

4.2 Control Interface

The CE implements an I^2C slave which is used as a control interface for commands and telemetry. It supports standard-mode (100 kHz) and fast-mode (400 kHz), as well as 3.3 V or 5 V signal levels. The 7-bit slave address is configurable, as well as the optional pull-up resistors.

The CE also provides a Serial-Peripheral Interface (SPI), which may be accessed via any available GPIO pins (see section 4.4). Also, the control electronics includes dedicated transceivers on-board to make provision for options such as a CAN interface or an RS4-22/RS-485 interface.

Table 4-2: Control Interface Options

Interface	Details
I^2C	Standard
SPI	Standard
CAN	Optional
RS-422/RS-485	Optional
Customer Specific Interface	Optional

4.3 High-Speed Interface

The High-Speed Interface is used for dedicated high-speed transfers, where image data is read out to a payload processor or downlink transmitter. The interface uses an in-house streaming protocol and five LVDS pairs to provide a data output with a bit rate of up to 200 Mbit/s, as shown in Table 4-4.

Table 4-3: High-Speed Data Interface Characteristics

Characteristic	Value
LVDS Pairs	4 or 5 (1)
Clock Frequency	100 MHz
Data Alignment	Centred
Data Lanes	2
Data Lane Rate	SDR

(1) 4 LVDS pairs excluding flow control, 5 pairs including flow control.

The 100 MHz source-synchronous clock is centre aligned to the two single data rate (SDR) data lanes. The data lanes are synchronised to the free-running clock using a dedicated synchronisation signal. Optional flow control is also available in cases where the receiver needs to throttle the incoming data stream. Table 4-4 describes the role of the LVDS pairs in more detail. The details pin assignment of the interface is shown in section 5.2.

Table 4-4: High-Speed LVDS Description

Signal Name	Description	Direction
Clock	Clock	Output
Sync	Synchronisation	Output
D0	Data Lane 0	Output
D1	Data Lane 1	Output
RR	Flow Control (Receiver Ready)	Input

4.4 General Purpose and High-Speed Digital I/Os

The CE includes a total of 30 I/O lines at a 3.3 V signal level, which may be used as part of the standard configuration or customer-specific interfaces (optional). These are essentially pins that are directly connected to the FPGA. All of these I/Os may be configured as single-ended general-purpose I/Os (GPIOs), while select I/Os maybe be configured as LVDS (differential) pairs for use as High-Speed I/Os (HSIOs). A total of 7 LVDS pairs are available to allow for customer-specific interfaces to be implemented. The available I/Os are summarised in Table 4-5. They are all located on the PC-104 connectors, with pin assignments described in 5.1.

Table 4-5: GPIOs and HSIOs

Description	Number
Total I/Os	30
GPIOs	Up to 30 (1)
HSIOs (LVDS pairs)	7

(1) The number of GPIOs available is reduced by 2 for each HSIO pair used.

When the SPI interface is selected, 4 GPIO lines must be reserved for this interface. GPIOs are also typically used as outputs to indicate a specific status or event (optional).

4.5 Telemetry and Health Monitoring

The CE provides comprehensive telemetry and health monitoring, with 32 unique measurement channels available, as shown in Table 4-6. The health monitoring allows for thorough analysis and fault-detection of the electronics while in-flight.

Table 4-6: Telemetry Measurement Channels

Sub-Circuit	Channel Description	Number of Channels
FEE	Supply Voltages	2
	Bias Voltages	8
	Sensor Temperature	1
CE Power Regulation	Supply Voltages	10
	Supply Currents	7
CE FPGA	Chip Temperature	1
	Supply Voltages	3
TOTAL		**32**

5. Electrical Interfaces

The HyperScape100 Control Electronics features two connectors for external interfacing – a standard CubeSat Kit Bus (CSKB) PC-104 connector pair (H1 and H2) and a custom high-density connector (P5) for high-speed data transfers. The pin assignment of the PC-104 connectors are not completely fixed, and many configuration selections are available to ease integration with existing systems. It is typically used for power supply and a control interface. High-speed data transfers (of image data) are recommended via connector P5. Connectors P2, P3 and P4 provide an internal interface to the FEE.

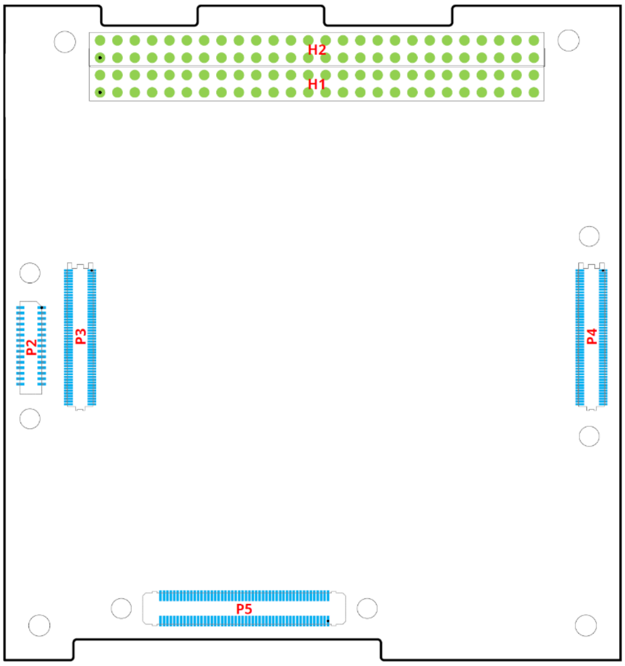

Figure 5-1: CE Connector Locations

5.1 CSKB PC-104 Connector H1 and H2

The standard CubeSat Kit Bus Connectors (H1 and H2) have a pin assignment as shown in Table 5-1 and Table 5-2. It should be noted that due to the diverse configuration selections, several pins appear in the table more than once, according to their configured role.

Table 5-1: Connector H1 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
47, 49, 51	5V_IN	Power	5 V Input Power supply (1)
4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16	PowerCtrl	3.3 V Input (2)	Power switch user control. High for on, low for off. (3)
1	CANL	CAN	Low level CAN bus line (5)
3	CANH	CAN	High level CAN bus line (5)
23, 41	SDA	3.3 V I/O (4)	I^{2}C serial data

Pin Number(s)	Pin Name	Signal Type	Description
21, 43	SCL	3.3 V Input (4)	I^2C serial clock
1, 2, 3, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 30, 31, 33, 40	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 29, 32, 35, 39	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 5 pairs)
12, 25, 26, 27, 28, 34, 36, 37, 38, 42, 44, 45, 46, 48, 50, 52	NC	N/A	Not connected.

Table 5-2: Connector H2 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
13, 15, 16, 25, 26	5V_IN	Power	5 V Input Power supply (1)
29, 30, 32	5V_RETURN	Power	5 V Power return
17, 18, 19, 20	PowerCtrl	3.3 V Input (2)	Power switch user control. High for on, low for off (3)
47	RS422_RX_A	RS-422	RS-422 Receiver A line (5)
49	RS422_RX_B	RS-422	RS-422 Receiver B line (5)
48	RS422_TX_A	RS-422	RS-422 Transmitter A line (5)
50	RS422_TX_B	RS-422	RS-422 Transmitter A line (5)
21, 22, 47, 48, 49, 50	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
17, 18, 19, 20, 47, 50	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 2 pairs)
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 23, 24, 27, 28, 31, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 51, 52	NC	N/A	Not connected.

(1) At least one 5 V power supply pin must be used, the rest may remain unconnected (as per the product configuration).
(2) PowerCtrl input is 5 V tolerant.
(3) Only one of these pins may be selected (as per the product configuration).
(4) I^2C interface may be configured for 5 V signal levels (as per the product configuration).
(5) Only available as an option

5.2 High-Speed Connector P5

The primary purpose of the high-density connector P5 is to provide an interface suitable for high-speed data transfers. A total of 9 LVDS pairs are available, but only 5 are used for the High-Speed Data interface, as described in 4.3. These LVDS pairs may also be used to implement a customer-specific interface if required, as a custom option. The connector also provides an alternate power and control (I^2C) interface.

Table 5-3: Connector P5 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 49, 50, 55, 56, 61, 62, 67, 68, 73, 74, 79, 80, 85	GND	Power	Digital Ground
93, 95, 96, 97, 98, 99, 100	5V_IN	Power	5 V Input Power supply
86, 89, 90, 91, 93, 94	5V_RETURN	Power	5 V Power return
87	PowerCtrl	3.3 V Input (1)	Power switch user control. High for on, low for off.
59	CE_On	3.3 V Output	Power Status. High when CE is on, low when off.
88	SDA	3.3 V I/O (2)	I^2C serial data
92	SCL	3.3 V Input (2)	I^2C serial clock
58	LVDS0_P	LVDS	High-speed LVDS, Clock+ (3)
60	LVDS0_N	LVDS	High-speed LVDS, Clock- (3)
64	LVDS1_P	LVDS	High-speed LVDS, Sync+ (3)
66	LVDS1_N	LVDS	High-speed LVDS, Sync- (3)
69	LVDS2_P	LVDS	High-speed LVDS, D0+ (3)
71	LVDS2_N	LVDS	High-speed LVDS, D0- (3)
70	LVDS3_P	LVDS	High-speed LVDS, D1+ (3)
72	LVDS3_N	LVDS	High-speed LVDS, D1- (3)
75	LVDS4_P	LVDS	High-speed LVDS, RR+ (3)
77	LVDS4_N	LVDS	High-speed LVDS, RR- (3)
76	LVDS5_P	LVDS	High-speed LVDS.
78	LVDS5_N	LVDS	High-speed LVDS.
81	LVDS6_P	LVDS	High-speed LVDS.
83	LVDS6_N	LVDS	High-speed LVDS.
82	LVDS7_P	LVDS	High-speed LVDS.
84	LVDS7_N	LVDS	High-speed LVDS.
63	LVDSaux_P	LVDS	High-speed LVDS.
65	LVDSaux_N	LVDS	High-speed LVDS.
3, 4, 5, 6, 9, 10, 11, 12, 15, 16, 17, 21, 22, 23, 24, 27, 28, 29, 30, 33, 34, 35, 36, 39, 40, 41, 42, 45, 46, 47, 48, 51, 52, 53, 54, 57	Reserved	N/A	Reserved

(1) PowerCtrl input is 5 V tolerant
(2) I^2C interface may be configured for 5 V signal levels (as per the product configuration sheet)
(3) LVDS assignments for standard High-Speed Data Interface

6. Electrical Specifications

6.1 Absolute Maximum Ratings

The absolute maximum ratings of the electrical interfaces are shown in Table 6-1. Use of the HyperScape100 beyond the absolute maximum ratings may cause permanent damage.

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
Power Supply				
V_{in}	5 V Input Supply	4.5	5.5	V
GPIOs (1)				
V_{GPIO}	Voltage on input/output pin	- 0.5	3.8	V
I^2C				
V_{I2C}	Voltage on I^2C pin	- 0.5	7	V
LVDS (2)				
V_{ICM}	Common-mode input voltage	0.6		V
V_{ID}	Differential input voltage	0.1		V
Power Control				
V_{PC}	High-level input voltage	0	5.0	V

(1) GPIOs include the SPI interface
(2) LVDS signals include the HSIOs and High-Speed Data Interface

6.2 Interface Specifications

The recommended signal levels for the Control Electronics interfaces are given in Table 6-2

Table 6-2: DC Signal Level Specifications

Symbol	Parameter	Min.	Typ.	Max.	Units
Power Supply					
V_{in}	5 V Input Supply	4.75	5.0	5.25	V
GPIOs (1)					
V_{IH}	High-level input voltage	2.0	-	3.45	V
V_{IL}	Low-level input voltage	- 0.3	-	0.8	V
V_{OH}	High-level output voltage	2.9	-	-	V
V_{OL}	Low-level output voltage	-	-	0.4	V
I_{SINK}, I_{SOURCE}	Current sink or source per pin	-	-	±10	mA
I^2C					
$V_{IH\ (5.0\ V)}$	High-level input voltage @ 5.0 V (3)	2.31	-	5.5	V
$V_{IH\ (3.3\ V)}$	High-level input voltage @ 3.3 V (3)	2.31	-	3.45	V
V_{IL}	Low-level input voltage	-0.5	-	0.99	V
V_{OL}	Low-level output voltage	-	0.1	0.2	V
LVDS (2)					
V_{ICM}	Common-mode input voltage	0.6	1.25	2.35	V
V_{ID}	Differential input voltage	0.1	0.35	0.6	V

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{OCM}	Common-mode output voltage	1.125	1.2	1.375	V
V_{OD}	Differential output voltage	0.25	0.35	0.45	V
Power Control					
V_{IH}	High-level input voltage	2.5	3.3	5.0	V
V_{IL}	Low-level input voltage	0.0	-	0.5	V

(1) GPIOs include the SPI interface
(2) LVDS signals include the HSIOs and High-Speed Data Interface
(3) The maximum input voltage depends on the selected I²C voltage (3.3 V or 5.0 V)

The AC characteristics of the interfaces are summarised in Table 6-3.

Table 6-3: AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
SPI					
f_{SPI}	SPI frequency	-	-	10	MHz
I²C					
f_{I2C}	I²C frequency	-	-	400	kHz
LVDS					
f_{LVDS}	LVDS frequency	-	100	-	MHz
Power Control					
t_{PULSE}	Input pulse width	100	-	-	ms

6.3 Power Consumption

The typical power consumption of the HyperSpace100, with a power supply of 5.0 V, is given below, for the beginning of life (BOL) as well as after exposure to radiation (total ionising dose of 25 krad).

Table 6-4: Power Consumption (BOL)

Operational Mode	Current (Typ.)	Power Consumption (Typ.)
Idle Mode (1)	470 mA	2.35 W
Imaging Mode (2)	1100 mA	5.50 W
Readout Mode (3)	470 mA	2.35 W

Table 6-5: Power Consumption (after 25 krad TID)

Operational Mode	Current (Typ.)	Power Consumption (Typ.)
Idle Mode (1)	495 mA	2.48 W
Imaging Mode (2)	1160 mA	5.80 W
Readout Mode (3)	495 mA	2.48 W

(1) CE is powered on, but the FEE is off. Control and High-Speed Data interfaces are static.
(2) CE and FEE are powered on, and an image is being captured.
(3) CE is powered on, but the FEE is off. Control and High-Speed Data interfaces are active.

7. Environmental Ratings

The HyperScape100 is designed for use in LEO orbit space applications, within the environmental conditions described in Table 7-1.

Table 7-1: Environmental Absolute Maximum Ratings

Description	Value
Operating Temperature	-10 to +50 °C
Survivable Temperature	-25 to +65 °C
Vibration	14.1 g_{rms} (all directions) (1)
Radiation (Total Ionizing Dose)	> 15 krad (2)

(1) Based on GSFC-STD-7000
(2) Performance guaranteed to 15 krad. Functional after 15 krad, but performance may be degraded.

8. Physical Characteristics

The physical characteristics of the HyperScape100 are shown in Table 8-1.

Table 8-1: Physical Characteristics

Description	Value
Mass	1.2 kg
Dimensions	98 x 98 x 176 mm

The mechanical drawing in Figure 8-1 below shows the independent mounting points of the OFE hardware and Figure 8-2 shows the standard PC-104 PCB mounting points of the control electronics. . All dimensions are in millimetres (mm).

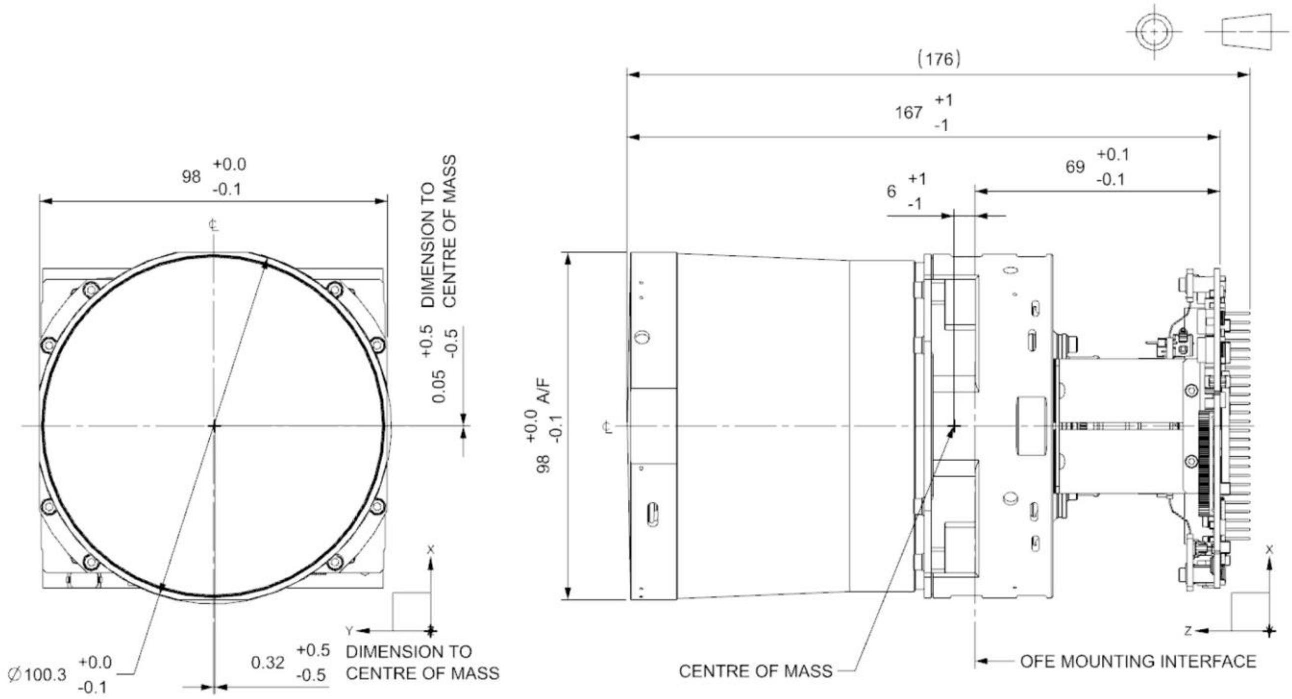

Figure 8-1: Mechanical Drawing

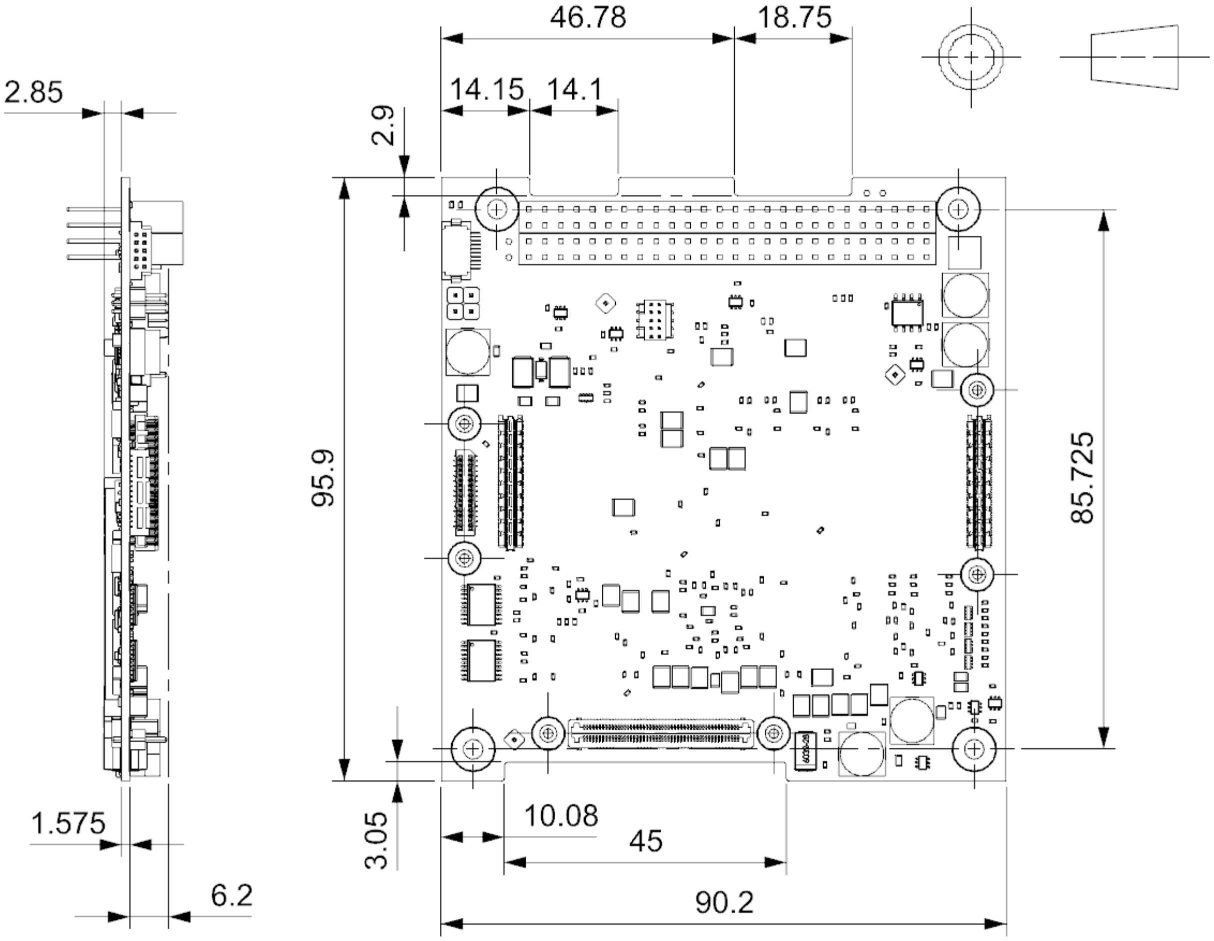

Figure 8-2: CE Mechanical Drawing

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HyperScape100

Interface Control Document

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Revision: 1

Controlled document note: It is the user's responsibility to verify that the revision of any printed documentation matches the configuration controlled revision.

Document History

Revision	Date	Details
1	2019-08-20	First release of document

Table of Contents

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List of Abbreviations

Abbreviation	Description
AIT	Assembly, Integration and Testing
BOL	Beginning of Life
CE	Control Electronics
CVCM	Collected Volatile Condensable Material
DC	Direct Current
FPGA	Field Programmable Gate Array
IO	Input/Output
ISO	International Organization for Standardization
LVDS	Low Voltage Differential Signalling
MSB	Most Significant Bit
NC	Not Connected
OFE	Optical Front-End
PCB	Printed Circuit Board
SPI	Serial Peripheral Interface
TML	Total Mass Loss

1. Introduction

1.1 Identification

Item Description: HyperScape100

Simera Item Number: SS100-034647

1.2 Intended Use

This document describes the interfaces and environmental conditions of the HyperScape100 Imager.

1.3 Context and Summary

The HyperScape100 is an electro-optical imaging system employing a CMOSIS CMV12000 sensor utilizing a linear variable filter. The HyperScape100 is produced by Simera Sense and is intended for earth observation applications. It is primarily designed to be implemented as part of an optical payload in a CubeSat. Its compact form factor allows for direct implementation into a 3U CubeSat structure; however, the HyperScape100 can also be used as part of larger satellite systems.

This Interface Control Document identifies, defines and describes the interfaces between the HyperScape100 and the surrounding satellite components, as well as between the HyperScape100 and its environment.

2. Referenced Documents

Table 2-1 lists documents that are referenced in this document. In the event of conflict between the contents of the reference documents and this document, this document shall take precedence.

Table 2-1: Referenced Documents

Ref. #	Reference
[1]	Outgassing Data for Selecting Spacecraft Materials. [Online]. Available: https://outgassing.nasa.gov/ [2018, October 24]
[2]	NXP I2C-bus specification and User Manual. [Online]. Available: https://www.nxp.com/docs/en/user-guide/UM10204.pdf [2018, October 24]

For undated references, the latest released version of the reference document applies. For dated references, subsequent versions of the document do not apply. It is best practice to always refer to the latest released version. Unless otherwise stated, web links referenced above were last accessed at the release date of the current version of this document.

3. System Description and Context

The HyperScape100 captures electromagnetic radiation, focuses the radiation on a sensor and converts the focused electromagnetic radiation into electrical signals. The HyperScape100 typically forms part of the payload of a satellite and is shown in the context of a typical CubeSat diagram in Figure 3-1 below.

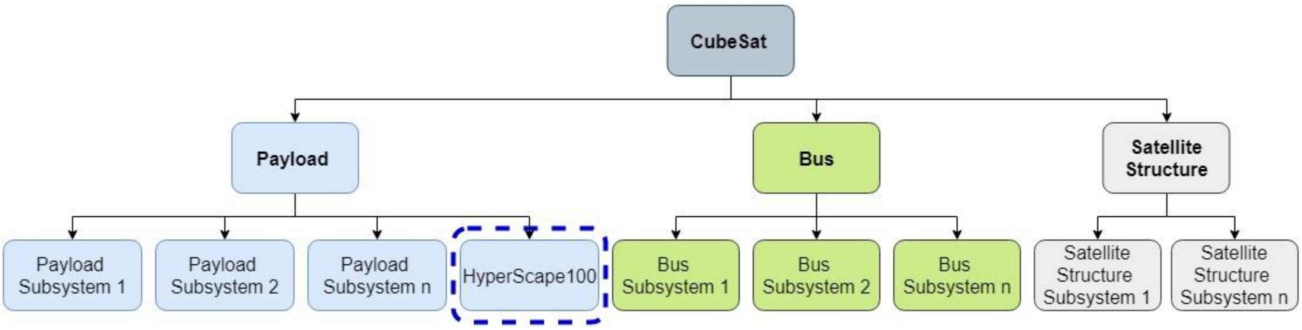

Figure 3-1: Typical CubeSat System Diagram

3.1 Physical Description

The HyperScape100, hereafter referred to as the "Imager", consists of several subassemblies which comprises of the xScape100 Optical Front-End (OFE), the HyperScape100 Sensor Unit and the HyperScape100 Control Electronics. Table 3-1 provides a functional description of the Imager and its components

Table 3-1 System and Component Functional Description

ID	Imager/Component	Primary Function
1	HyperScape100	Collects electromagnetic radiation and converts it into electrical signals
1.1	xScape100 OFE	Focuses the collected electromagnetic radiation onto an imaging sensor
1.2	HyperScape100 Sensor Unit	Positions the sensor on the focal plane and converts the focused electromagnetic radiation into electrical signals
1.3	HyperScape100 Control Electronics	Powers and drives the sensor unit, as well as provides storage space for the captured images

Figure 3-2 illustrates the physical system subassemblies and provides the axis definition.

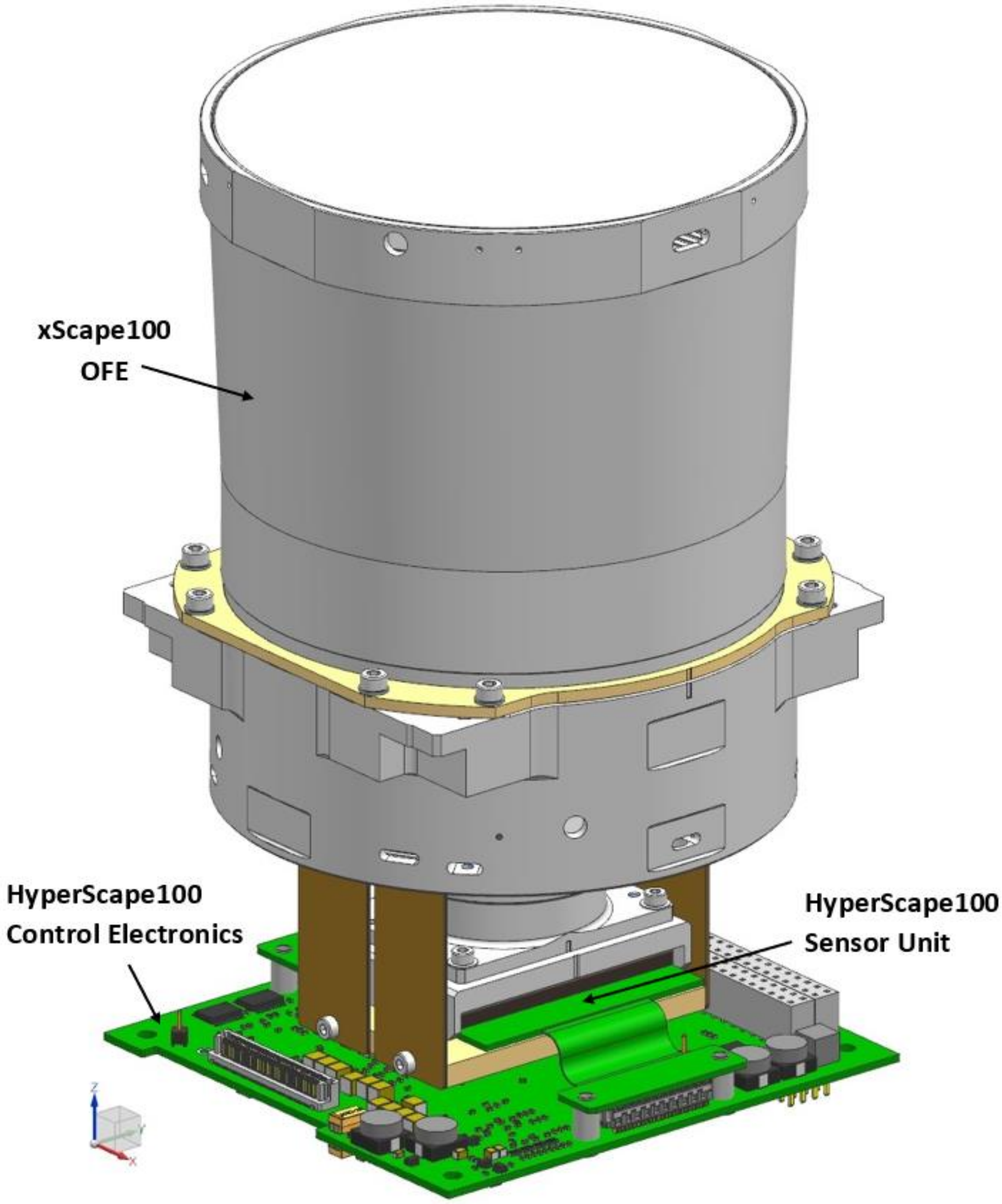

Figure 3-2: HyperScape100 with Axis Definition

3.2 Physical Properties

The physical properties of the Imager are presented in Table 3-2. The reference axis system used to define the moments of inertia and centre of mass position is located at the geometric centre of the OFE's mounting points which is shown in Figure 4-2.

Table 3-2: Physical Properties

Property	Unit	Value
Mass	kg	1.14 (± 5%)
Moments of Inertia		
I_{xx}	$kg.m^2$	3.70E-03 (± 5%)
I_{yy}	$kg.m^2$	3.65E-03 (± 5%)
I_{zz}	$kg.m^2$	1.55E-03 (± 5%)
Centre of Mass		
x	mm	< 0.5 (± 0.5) See Figure 3-3
y	mm	< 0.5 (± 0.5) See Figure 3-3
z	mm	7 (± 1) See Figure 3-3

Table 3-3 provides the natural frequencies of the Imager (from 0 - 2000 Hz) when it is rigidly constrained at its four mounting points which is shown in Figure 4-2.

Table 3-3: Natural Frequencies of the Imager from 0 – 2000 Hz

Mode Number	Frequency [Hz]
1	684
2	705
3	800
4	854
5	891
6	996
7	1020
8	1072
9	1157
10	1587
11	1691
12	1718
13	1820
14	1839
15	1855
16	1933
17	1947
18	1997

Figure 3-3 presents the envelope dimensions of the Imager and indicates the position of the centre of mass relative to the OFE's mounting points.

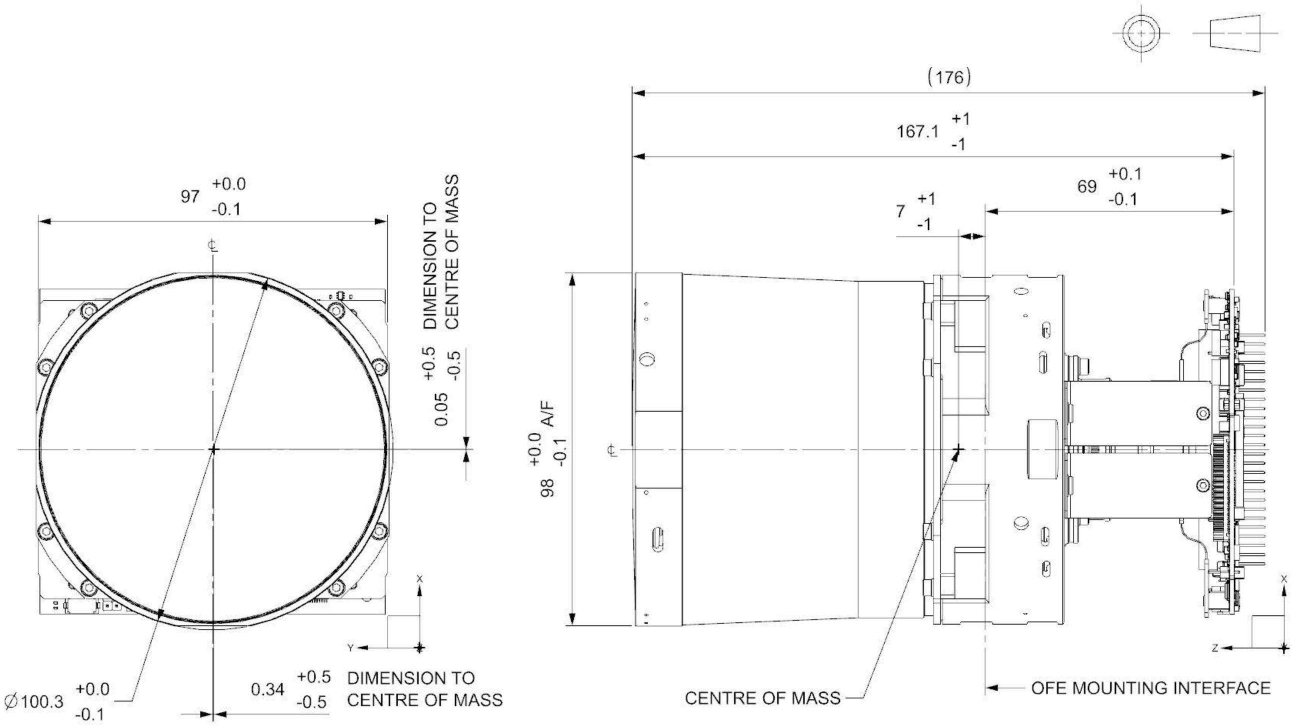

Figure 3-3: Centre of Mass Position

4. Description of System Interfaces

4.1 Interface Identification and Definition

The various interfaces between the Imager and the satellite components, as well as between the Imager and its environment, are shown graphically in Figure 4-1 below. The satellite components are herein defined as being all components which do not form part of the Imager and as such includes the satellite structure.

Note: For analysis purposes it is assumed that there is no thermal interface via the wiring harnesses.

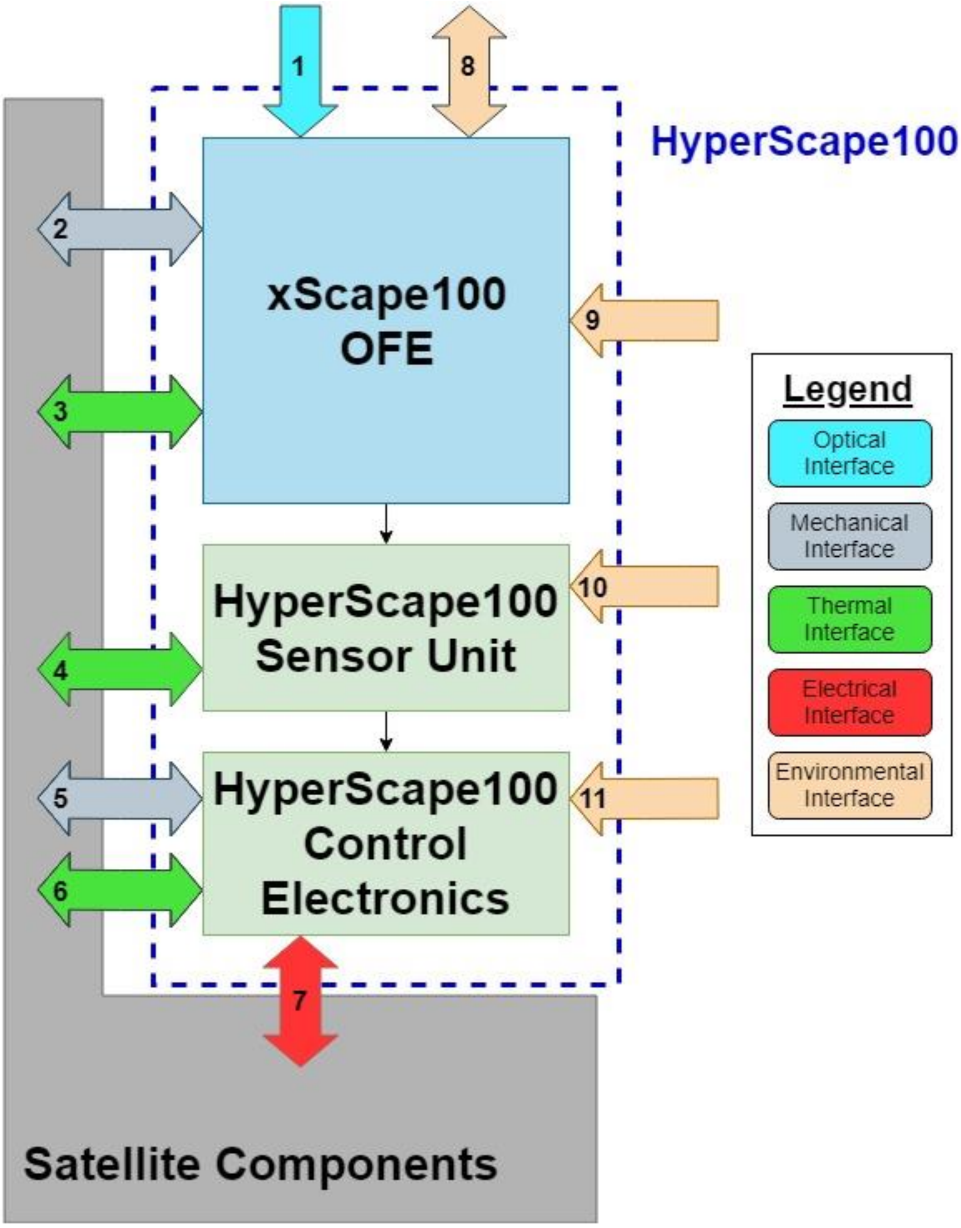

Figure 4-1: Interface Identification Diagram

The interfaces identified in Figure 4-1, are defined in Table 4-1 below. The descriptions of the interfaces are presented in the subsections following Figure 4-1.

Table 4-1: Interface Definition

Interface Number	Interface Type	Interface From	Interface To
1	Optical	Target in View	xScape100 OFE
2	Mechanical	xScape100 OFE	Satellite Components
3	Thermal	xScape100 OFE	Satellite Components
4	Thermal	HyperScape100 Sensor Unit	Satellite Components
5	Mechanical	HyperScape100 Control Electronics	Satellite Components
6	Thermal	HyperScape100 Control Electronics	Satellite Components
7	Electrical (Power and Control)	Satellite Components	HyperScape100 Control Electronics
8	Environmental (Thermal Radiation)	xScape100 OFE	Environment
9	Environmental (Cosmic Radiation)	Environment	xScape100 OFE
10	Environmental (Cosmic Radiation)	Environment	HyperScape100 Sensor Unit
11	Environmental (Cosmic Radiation)	Environment	HyperScape100 Control Electronics

4.2 Optical Interface

4.2.1 Interface 1: Target in View to xScape100 OFE

The xScape100 OFE has an optical interface at its front aperture with a diameter 95 mm and a full field of view of 2.96 degrees. The function of this interface is to enable the collection of electromagnetic radiation by the OFE. This optical interface shall remain unobscured during imaging to ensure optimal performance of the Imager.

4.3 Mechanical Interfaces

4.3.1 Interface 2: xScape100 OFE to Satellite Components

The OFE interfaces mechanically with the satellite structure via four threaded mounting points which are located on the OFE. The function of this interface is to secure the OFE to the applicable satellite components and act as the main structural support for the Imager.

The mating interface which is bolted to the OFE shall have four through holes with a diameter of 3.4 mm or larger. These through holes shall be spaced to match the hole spacing of the four M3 threaded holes (as shown in Figure 4-2) exactly and shall have a positional tolerance of 0.1 mm. In addition, all interfaces which mate directly to the mounting interface of the OFE shall have a flatness tolerance of 50 µm or smaller and shall have a N7 surface finish (this is equivalent to a surface finish with an average roughness of R_a = 1.6 µm).

Caution shall be exercised during the assembly of any mechanics to the mounting interface of the OFE. Any mechanics which must be mounted to the OFE, shall first be secured to the OFE's mounting interface, only then shall the mechanics be joined to the rest of the satellite structure. This shall be done to ensure that the mounting surfaces of the OFE remain coplanar in the z-direction. Figure 4-2 provides the dimensions of the OFE's mounting interface.

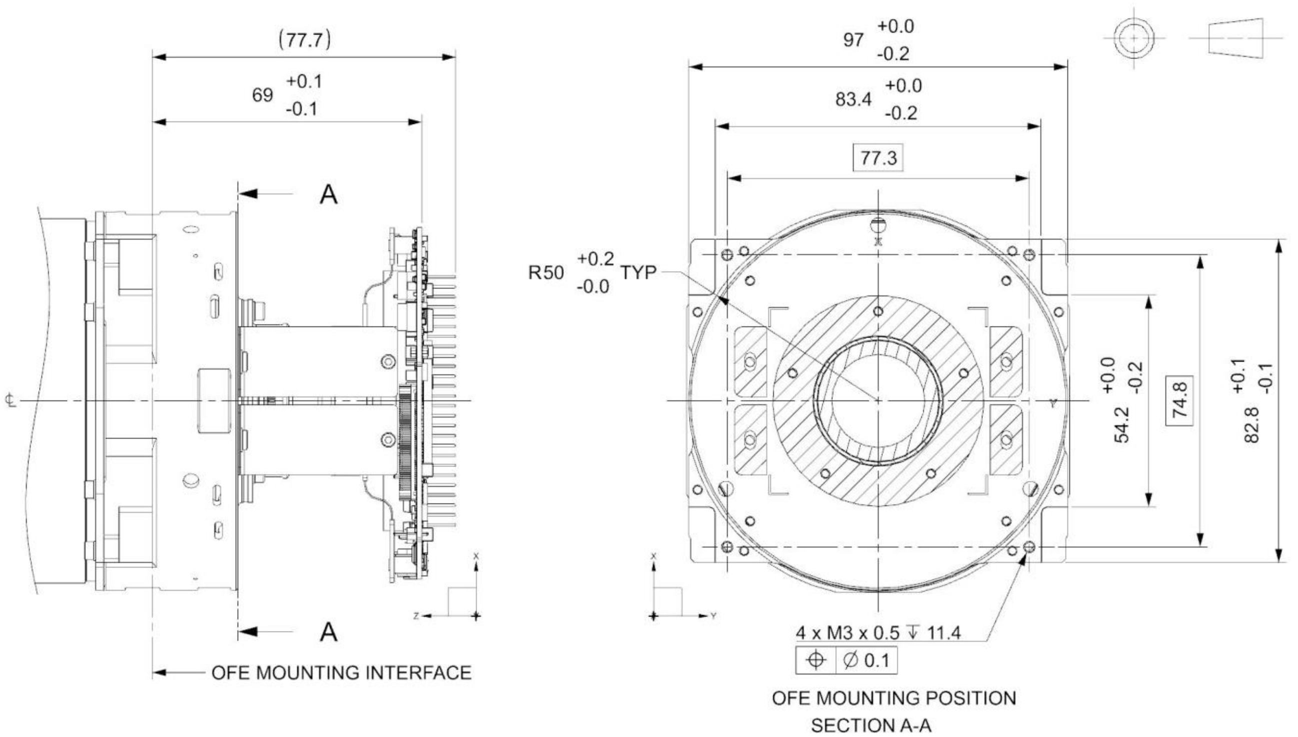

Figure 4-2: OFE Mounting Interface Dimensions

The details of the mounting interface are specified in Table 4-2 below.

Table 4-2: OFE Mounting Interface Specifications

Description	Value
Interface Material	Titanium Grade 5 (Ti-6Al-4V)
Interface Surface Finish	Bare Ti-6Al-4V, N7 surface finish
Flatness	<20 µm
Number of Mounting Locations	4
Thread Specification	M3 x 0.5 (see Figure 4-2)
Depth of Thread Supplied in OFE	11.4 mm
Fastener Torque (for stainless steel A4-70 fastener material). All fasteners shall be staked using Scotch Weld EC2216 adhesive or equivalent.	1 Nm

4.3.2 Interface 5: HyperScape100 Control Electronics to Satellite Components

The HyperScape100 Control Electronics (CE) interfaces mechanically with the satellite components through the four mounting holes located on the edges of the printed circuit board (PCB). These four mounting holes are through holes in the PCB and their spacing conforms to the PC-104 standard. The function of this interface is to secure the PCB to the applicable satellite component and act as main structural support for the CE. Figure 4-3 displays the dimensions of the CE PCB, as well as the height of the components on both sides of the PCB.

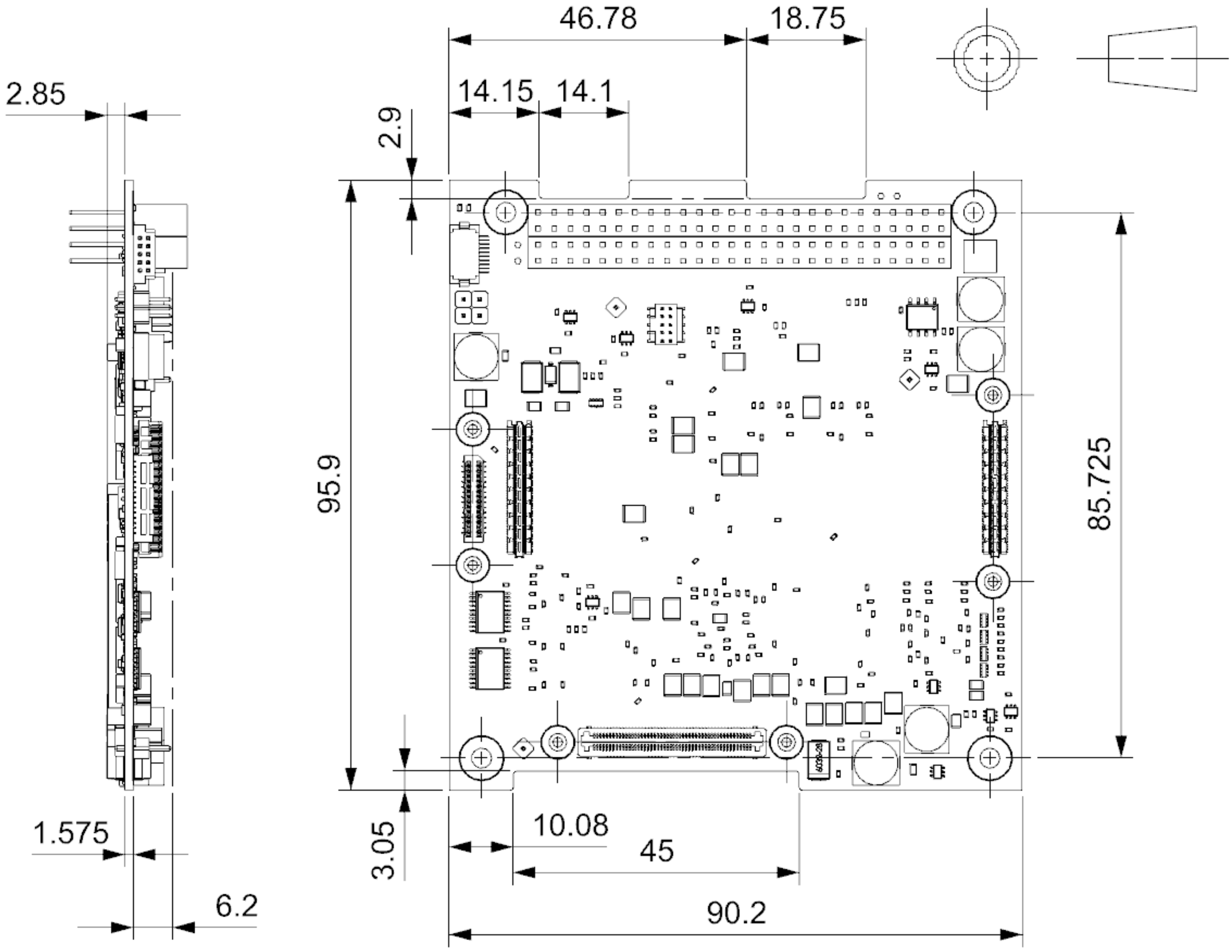

Figure 4-3: CE Mechanical Drawing

In Figure 4-4 below, the mounting details of the CE, as well as of the high-speed connector on the CE PCB are shown in more detail.

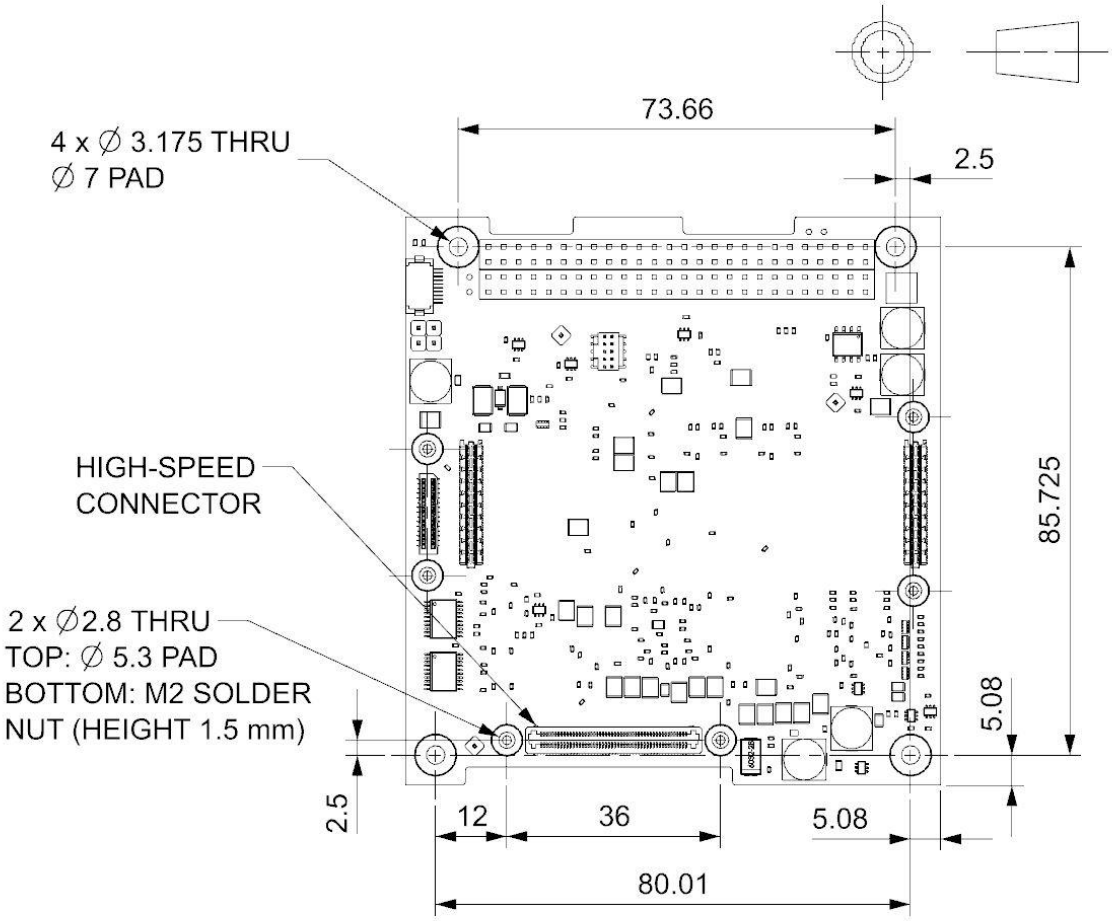

Figure 4-4: CE and High-Speed Connector Mounting Hole Details

Figure 4-5 shows the mounting position of the CE relative to the OFE.

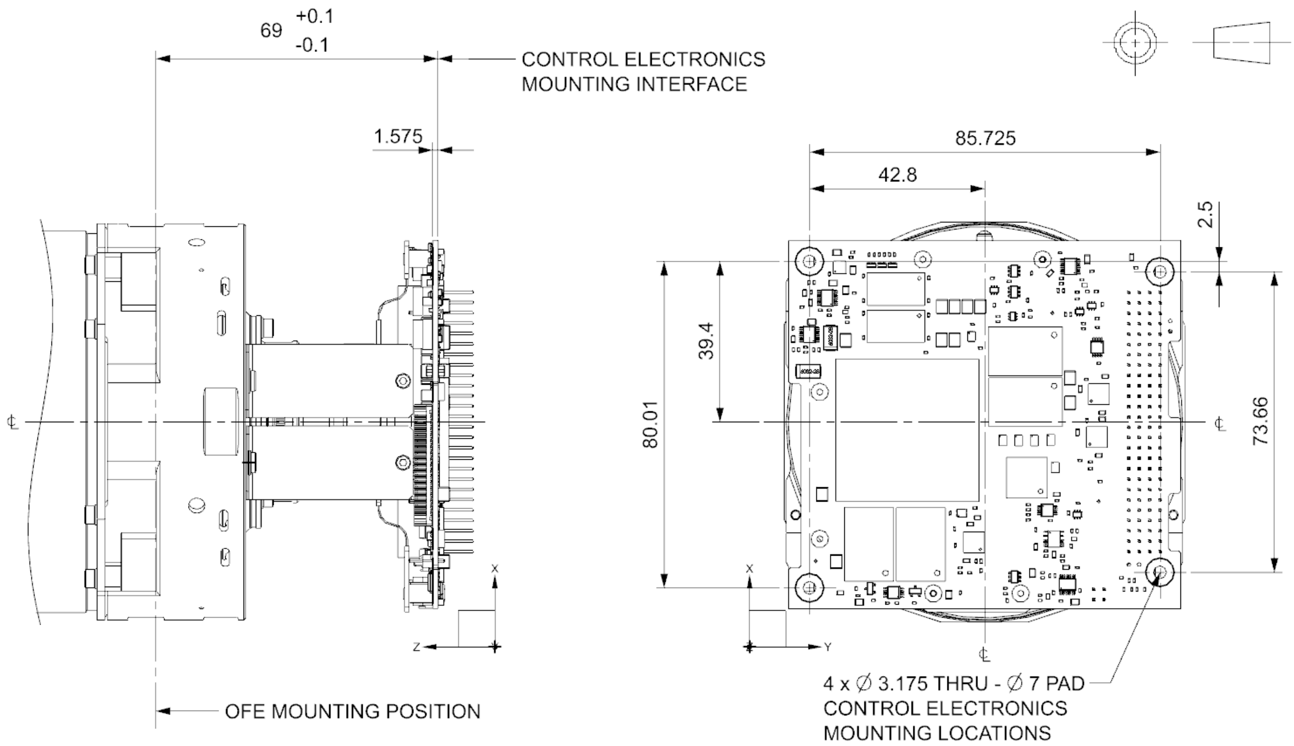

Figure 4-5: CE Mounting Position Relative to OFE

4.4 Thermal Interfaces

4.4.1 Interface 3: xScape100 OFE to Satellite Components

The mounting interface between the OFE and applicable satellite components facilitates heat transfer through thermal conduction between the OFE and the satellite components. In addition, thermal energy is also exchanged (by means of radiation) between the OFE and the surrounding satellite components. No specific requirement is placed on the amount of energy transmitted via conduction and radiation.

4.4.2 Interface 4: HyperScape100 Sensor Unit to Satellite Components

Thermal energy is exchanged by means of radiation between the HyperScape100 Sensor Unit and the surrounding satellite components. No specific requirement is placed on the amount of energy transmitted via radiation.

4.4.3 Interface 6: HyperScape100 Control Electronics to Satellite Components

The mounting points of the CE facilitates heat transfer through thermal conduction between the CE and the surrounding satellite components. In addition, thermal energy is also exchanged (by means of radiation) between the CE and the surrounding satellite components. No specific requirement is placed on the amount of energy transmitted via conduction and radiation.

4.5 Electrical Interfaces

4.5.1 Interface 7: Satellite Components to HyperScape100 Control Electronics

This interface consists of a single or of multiple electrical connector(s) to act as interface between the CE and the applicable satellite component(s). The function of this interface is to transmit power, control and data to and from the CE.

4.5.1.1 PC-104 Interface

The CE supports a CubeSat Kit Bus compatible PC-104 header and its pin description is given in Figure 4-6.

H1

	CANL *	IO0	1	2	IO1		
	CANH *	IO2	3	4	IO3	PowerCtrl	LVDS6-
LVDS6+	PowerCtrl	IO4	5	6	IO4	PowerCtrl	LVDS6+
LVDS7+	PowerCtrl	IO5	7	8	IO5	PowerCtrl	LVDS7+
LVDS7-	PowerCtrl	IO6	9	10	IO6	PowerCtrl	LVDS7-
LVDS3-	PowerCtrl	IO7	11	12	*NC*		
LVDS3+	PowerCtrl	IO8	13	14	IO8	PowerCtrl	LVDS3+
	PowerCtrl	IO9	15	16	IO9	PowerCtrl	
		IO10	17	18	IO10		
		IO11	19	20	IO11		
	SCL	IO12	21	22	IO12		
	SDA	IO13	23	24	IO13		
		NC	25	26	*NC*		
		NC	27	28	*NC*		
LVDS5-		IO14	29	30	IO15		
		IO16	31	32	IO17		LVDS5+
		IO18	33	34	*NC*		
LVDS2-		IO19	35	36	*NC*		
		NC	37	38	*NC*		
LVDS2+		IO20	39	40	IO21		
	SDA	IO22	41	42	*NC*		
	SCL	IO23	43	44	*NC*		
		NC	45	46	*NC*		
		5V	47	48	*NC*		
		5V	49	50	*NC*		
		5V	51	52	*NC*		

H2

		NC	1	2	*NC*		
		NC	3	4	*NC*		
		NC	5	6	*NC*		
		NC	7	8	*NC*		
		NC	9	10	*NC*		
		NC	11	12	*NC*		
		5V	13	14	*NC*		
		5V	15	16	5V		
LVDS4-	PowerCtrl	IO24	17	18	IO24	PowerCtrl	LVDS4-
LVDS4+	PowerCtrl	IO25	19	20	IO25	PowerCtrl	LVDS4+
		IO26	21	22	IO26		
		NC	23	24	*NC*		
		5V	25	26	5V		
		NC	27	28	*NC*		
		GND	29	30	GND		
		NC	31	32	GND		
		NC	33	34	*NC*		
		NC	35	36	*NC*		
		NC	37	38	*NC*		
		NC	39	40	*NC*		
		NC	41	42	*NC*		
		NC	43	44	*NC*		
		NC	45	46	*NC*		
LVDS1-	RS422 A RX	IO27	47	48	IO28	RS422 A TX	
	RS422 B RX	IO29	49	50	IO30	RS422 B TX	LVDS1+
		NC	51	52	*NC*		

Figure 4-6: CubeSat Kit Bus Compatible PC-104 Header Schematic

The pins labelled '*NC*' are not connected on the CE. The rest of the pins are not connected by default and are configured through the product configuration sheet if and how they are connected. All pins labelled 'IOn' can be routed directly to a 3.3 V FPGA IO bank if their secondary function is not used. Those labelled 'LVDSn±' are routed differentially and can therefore be used as LVDS pairs. The 'IOn' pins can be used for SPI interfaces, or high speed LVDS point-to-point interfaces, or hard telecommands.

4.5.1.2 Power Interface

The CE requires a Direct Current (DC) supply regulated at 5 V ± 10% at a current of at least 1.5 A. The nominal Beginning of Life (BOL) DC current consumption for the different modes in the operational state is given in Table 4-3.

Table 4-3: Imager BOL Power Consumption

Operational Mode	Imager Current Consumption at 5 V nominal supply voltage	Imager Power Consumption
Idle Mode	500 mA	2.5 W
Imaging Mode	1200 mA	6.0 W
Readout Mode	500 mA	2.5 W

The 5 V supply must be supplied by one, or a combination, of H1.47, H1.49, H1.51, H2.13, H2.15, H2.16, H2.25, and H2.26, depending on the selections made in the product configuration sheet. The ground connection is made by one, or a combination, of H2.29, H2.30, and H2.32.

The CE has an optional power switch onboard that can be used to switch power to the Imager on. This may be used if the 5 V supplied to the CE is not switched. If this power switch is selected in the product configuration sheet, its control line “PowerCtrl” can be routed to one, or a combination, of H1.4, H1.5, H1.6, H1.7, H1.8, H1.9, H1.10, H1.11, H1.13, H1.14, H1.15, H1.16, H2.17, H2.18, H2.19 or H2.20, depending on the selections made in the product configuration sheet. The “PowerCtrl” control signal is active high. To turn on the CE, the “PowerCtrl” control signal must be driven high by applying a voltage between 2.5 V and 5.0 V for at least 100 ms.

The “PowerCtrl” signal may optionally be used to power the CE off (as well as on). If this option is selected the Imager can be turned off by driving “PowerCtrl” low to between 0 V and 0.5 V for at least 100 ms. This option can be enabled in the product configuration sheet. If this option is selected, the CE will power-cycle itself in the event of a radiation induced overcurrent condition.

The “PowerCtrl” signal may optionally be latched onboard the CE. If this option is enabled, the “PowerCtrl” signal may be deasserted after the CE has switched on which enables the CE to turn the Imager completely off in the event of a radiation induced overcurrent condition. This option can be enabled in the product configuration sheet. An unused “IOn” signal may be used as feedback and will be driven high when the imager is powered on and pulled to GND when the imager is turned off.

4.5.1.3 Control Interface

This interface is used to control the CE and receive telemetry from the CE. The control interface can be I²C or SPI and provides access to 32-bit registers. As such the control interface transfers are always 4 bytes long. The paragraphs that follow provide more information on the physical interface layers.

I²C Interface

The CE implements an I²C slave interface. Refer to [2] for the I²C-bus specification. The CE supports Standard-mode and Fast-mode as defined in [2]. Depending on the selections made in the product configuration sheet, the I²C Interface can operate at either 3.3 V or 5 V voltage levels and supports 7-bit slave addressing. Each transfer always contains 4 data bytes.

The SCL signal can be routed to either H1.21 or H1.43 and the SDA signal to either H1.23 or H1.41 depending on the selections made in the product configuration sheet. The SCL and SDA signals can optionally be pulled up to the bus voltage (3.3 V or 5 V as configured) if enabled in the product configuration sheet.

The I²C slave address is taken from the product configuration sheet.

SPI Interface

The CE implements a 3.3 V logic compatible SPI slave interface which consists of four signals. These four signals can be routed to any open "IOn" pin on the PC-104 Interface as defined in 4.5.1.1. The four SPI signals are:

- nSEL – Active low select signal generated by the master to select the slave interface. When not active (high) the SPI interface is not selected and placed in its reset state. All communication is initiated by the master first driving this nSEL signal low. It is kept low for the duration of the communication. It has a weak (± 20 kΩ) pullup resistor to 3.3 V.
- MOSI - Master Out Slave In signal is the data output of the master. It has a weak (± 20 kΩ) configurable pullup/pulldown resistor to 3.3 V/GND.
- MISO – Master In Slave Out is the data output of the slave. It has a weak (± 20 kΩ) pullup resistor to 3.3 V.
- SCK – The serial clock signal driven by the master. It has a weak (± 20 kΩ) pulldown resistor to GND. The maximum clock rate is 10 MHz.

The SPI interface conforms to the SPI standard "00" (clock polarity '0', clock phase '0'). As such the values on the MOSI and MISO lines are valid at the rising edge of SCK and remain valid until the next SCK shift edge. Refer to Figure 4-7 for the timing diagram.

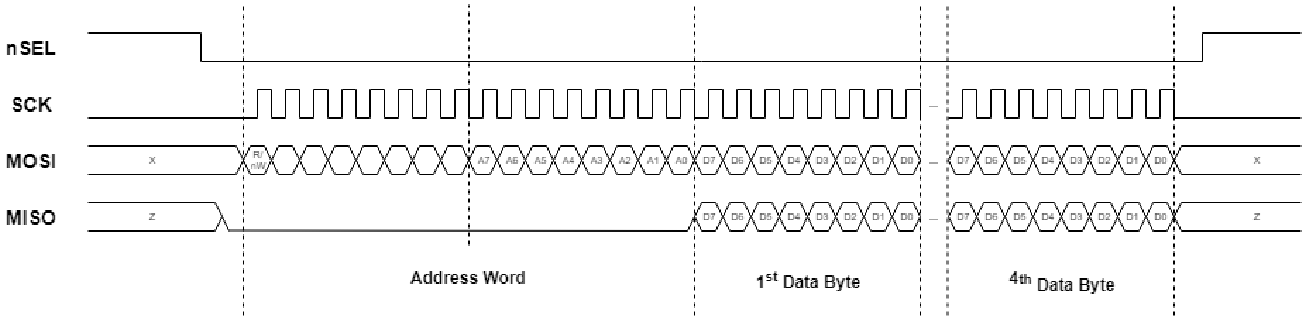

Figure 4-7: SPI Interface Timing Diagram

A transfer is initiated by the Address Word (16 bits) which specifies a read or write action as well as the register address. The CE echo's the received action and command bits on its MISO output while the master outputs them on the MOSI line. One or more bytes of data follows the command byte during which the CE MISO output may toggle depending on the action and command.

4.5.1.3.2 Connector Details

Two Samtec SSQ/ESQ Series connectors are used, one each for H1 and H2. The PC-104 connector is optional, and its fitment and choice of connector depends on the selections made in the product configuration sheet. Instead of fitting the connectors, wires may be soldered directly into the pads instead with adjacent pads used as strain relief.

4.5.1.4 High-Speed Data Interface

The CE provides a half-duplex bi-directional high-speed data interface consisting of up to eight LVDS pairs. The LVDS pairs are all bi-directional and are organised as shown in Table 4-4.

Table 4-4: High-Speed Data Interface Signal Assignment

Pair No.	Name	Description
1	Clock	Clock to which data is synchronised
2	D0	Data Lane 0
3	D1	Data Lane 1 (optional)
4	D2	Data Lane 2 (optional)
5	D3	Data Lane 3 (optional)
6	Sync/Valid	Signals first bit in transfer. Byte invalid if not asserted.
7	Flow Control	Return line to throttle data transfer (optional)
8	Reserved	

The optional additional data lanes D1 to D3 allow faster transmission or they may be repurposed to implement full duplex communication. Data is transmitted most significant bit (MSB) first. The signal timing diagram is shown in Figure 4-8.

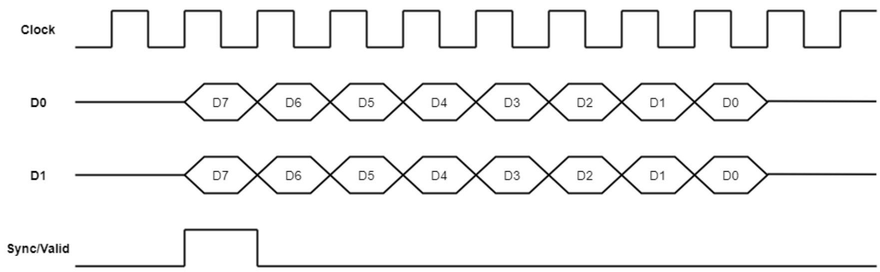

Figure 4-8: High-Speed Data Interface Timing Diagram

Transfers are always done in full bytes. The Sync/Valid signal indicates the MSB of the transfer. If it is not asserted at the beginning of the next byte, that transfer is deemed invalid and the byte transferred should be discarded. When multiple lanes are used, each lane transfers a full byte at the same time. The Sync/Valid signal is therefore applicable to all lanes.

The flow control signal is optional and can be used to throttle the data rate.

4.5.1.4.1 Connector Details

A Samtec LSHM-150-03.0-L-DV-A-N connector is used. A rendering of the connector is shown in Figure 4-9.

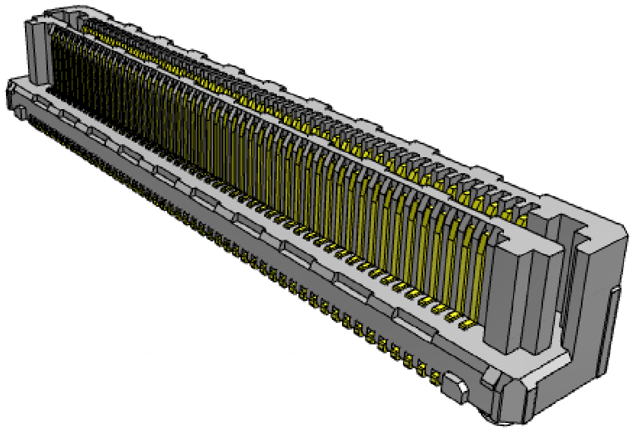

Figure 4-9: High-Speed Data Connector

The CE PCB has mounting holes either side of this connector that can be used to fasten the mating circuit to the CE. Details of the mounting holes are shown in Figure 4-4. The connector pinout is shown in Table 4-5. Do not connect to the pins labelled "Reserved". Pin 1 is located as per the recommended PCB layout prescribed by Samtec.

Table 4-5: High-Speed Data Connector Pinout

Pin No.	Signal	Pin No.	Signal
1	GND	2	GND
3	Reserved	4	Reserved
5	Reserved	6	Reserved
7	GND	8	GND
9	Reserved	10	Reserved
11	Reserved	12	Reserved
13	GND	14	GND
15	Reserved	16	Reserved
17	Reserved	18	Reserved
19	GND	20	GND
21	Reserved	22	Reserved
23	Reserved	24	Reserved
25	GND	26	GND
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	GND	32	GND
33	Reserved	34	Reserved
35	Reserved	36	Reserved
37	GND	38	GND
39	Reserved	40	Reserved
41	Reserved	42	Reserved
43	GND	44	GND
45	Reserved	46	Reserved
47	Reserved	48	Reserved
49	GND	50	GND
51	Reserved	52	Reserved
53	Reserved	54	Reserved
55	GND	56	GND
57	IO	58	Pair0+
59	Reserved	60	Pair0-
61	GND	62	GND
63	PairAux+	64	Pair1+
65	PairAux-	66	Pair1-
67	GND	68	GND
69	Pair2+	70	Pair3+
71	Pair2-	72	Pair3-
73	GND	74	GND
75	Pair4+	76	Pair5+
77	Pair4-	78	Pair5-
79	GND	80	GND
81	Pair6+	82	Pair7+
83	Pair6-	84	Pair7-

Pin No.	Signal
85	GND
87	GND
89	GND
91	Reserved
93	GND
95	Reserved
97	GND
99	Reserved

Pin No.	Signal
86	GND
88	GND
90	GND
92	Reserved
94	GND
96	Reserved
98	GND
100	Reserved

4.5.1.5 Earth Strap

All mounting holes on the CE are connected to each other and to GND through a single 22 ohm resistor to facilitate earth strapping.

4.6 Environmental Interfaces

4.6.1 Thermal Radiation Interface

4.6.1.1 Interface 8: xScape100 OFE to Environment

The front aperture of the OFE exchanges heat through thermal radiation with the space environment at the aperture. The function of this interface is to transmit thermal energy between the OFE and the space environment by means of radiation.

4.6.2 Cosmic Radiation Interfaces

4.6.2.1 Interface 9: Environment to xScape100 OFE

There is an interface between the space environment and the OFE through which cosmic radiation is transmitted to the OFE.

4.6.2.2 Interface 10: Environment to HyperScape100 Sensor Unit

There is an interface between the space environment and the HyperScape100 Sensor Unit through which cosmic radiation is transmitted to the sensor unit.

4.6.2.3 Interface 11: Environment to HyperScape100 Control Electronics

There is an interface between the space environment and the CE through which cosmic radiation is transmitted to the CE.

5. Environmental Requirements

5.1 Transportation

5.1.1 Temperature

During transportation and in a non-operating condition the maximum temperature of the Imager assembly shall not exceed 50 degrees Celsius.

During transportation and in a non-operating condition the minimum temperature of the Imager assembly shall not be less than -10 degrees Celsius.

5.1.2 Humidity

The humidity during transportation shall be less than 60%, non-condensing.

5.1.3 Vibration

All handling operations shall limit static accelerations to the complete Imager assembly to less than 5 g in all directions.

5.1.4 Shock

All handling operations shall limit shock exposure to the complete Imager assembly to less than 5 g maximum.

5.1.5 Cleanliness

During transportation the Imager shall be kept in an environment with a cleanliness of at least International Organization for Standardization (ISO) level 8 as per ISO 14644-1:2015 standards.

5.2 Storage

During storage it will be assumed that the Imager will not be in motion, therefore vibration and shock loading conditions are not relevant. During storage the following conditions must be adhered to:

5.2.1 Temperature

During prolonged storage and in a non-operating condition the maximum temperature shall not exceed 30 degrees Celsius.

During prolonged storage and in a non-operating condition the minimum temperature shall not be less than 10 degrees Celsius.

5.2.2 Humidity

The humidity during prolonged storage shall be between 30% and 60%, non-condensing.

5.2.3 Cleanliness

During prolonged storage the Imager shall be kept in an environment with a cleanliness of at least ISO level 8, as per ISO 14644-1:2015 standards, or better.

5.3 Assembly, Integration and Testing

All Assembly, Integration and Testing (AIT) procedures must be performed in an ISO class 8 cleanroom, as per ISO 14644-1:2015 standards, or equivalent. In addition, during AIT the following conditions shall always be adhered to:

5.3.1 Vibration

All handling operations shall limit static accelerations to the complete Imager assembly to less than 5 g in all directions.

5.3.2 Shock

All handling operations shall limit shock exposure to the complete Imager assembly to less than 5 g maximum.

5.3.3 Mechanical Interface with OFE

During all assembly and integration procedures, all mechanical mating interfaces with the OFE shall cause zero relative displacement (in the x and y directions) between any of the OFE's four mounting points.

5.4 In-Orbit

5.4.1 Survivable Temperature

In order to ensure survival, the maximum temperature of the Imager shall not be greater than 65 degrees Celsius and the minimum temperature shall not be less than -25 degrees Celsius.

5.4.2 Operating Temperature

During operation the maximum temperature of the Imager shall not exceed 50 degrees Celsius and the minimum temperature shall not be less than -10 degrees Celsius.

5.4.3 Operating Temperature Gradients

During operation the maximum axial temperature gradient over the OFE shall not be greater than 3 degrees Celsius.

During operation the maximum transverse temperature gradient over the OFE shall not be greater than 2 degrees Celsius.

5.4.4 Outgassing of Satellite Components

Material used in satellite components, which are near the Imager, shall have a maximum Total Mass Loss (TML) of less than 1.0% and a maximum Collected Volatile Condensable Material (CVCM) of less than 0.10%. Refer to [1] for a list of material TML and CVCM data.

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